OPA375 500-µV (Maximum), 10-MHz, Low Broadband Noise, RRO, Operational Amplifier

1 Features

- Low Broadband Noise: 3.7 nV/√Hz
- Low Offset Voltage: 500 µV (Maximum)
- Gain Bandwidth: 10 MHz
- Low Input Bias Current: 10 pA
- Rail-to-Rail Output
- Unity-Gain Stable
- Low I_Q: 890 µA/ch
- Microsize Package: SC70 (DCK)
- Wide Supply Range: 2.25 V to 5.5 V
- ESD Protection: ±3000 V Human Body Model (HBM)

2 Applications

- Photodiode Amplifiers
- Precision Sensor Front-Ends
- ADC Input-Driver Amplifiers
- Test and Measurement Equipment
- Sensor Field Transmitters
- Wearable Consumer Applications
- Audio Equipment
- Medical Instrumentation
- Active Filters

3 Description

The OPA375 operational amplifier (op amp) is a general-purpose CMOS op amp that provides low noise of 3.7 nV/√Hz. low offset of 500µV (maximum) and a wide bandwidth of 10 MHz. The low noise and wide bandwidth make the OPA375 device attractive for a variety of precision applications that require a good balance between cost and performance. Additionally, the input bias current of the OPA375 supports applications with high source impedance.

The robust design of the OPA375 provides ease-of-use to the circuit designer due to the unity-gain stability, integrated RFI/EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (1-kV HBM). Additionally, the resistive open-loop output impedance allows for easy stabilization with much higher capacitive loads.

This op amp is optimized for low-voltage operation as low as 2.25 V (±1.125 V) and up to 5.5 V (±2.75 V), and is specified over the temperature range of –40°C to +125°C.

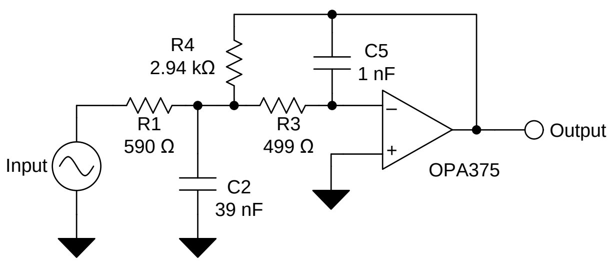
The single-channel OPA375 is available in a small-size SC70-5 package.

Device Information (1)

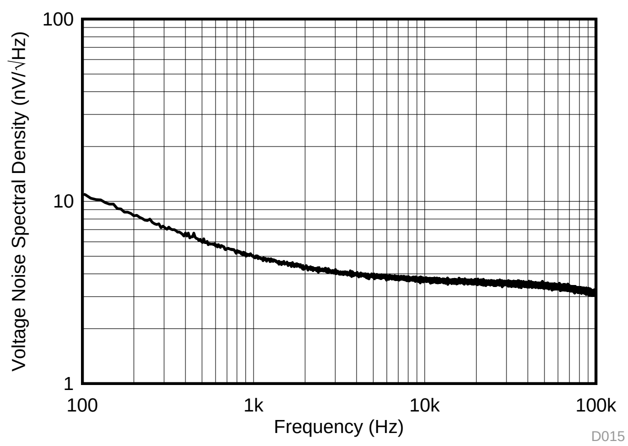
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA375	SC70 (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

OPA375 in a Low-Pass Filter Application



Noise Spectral Density vs Frequency



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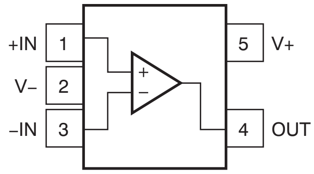
4 Revision History

DATE	REVISION	NOTES
November 2017	*	Initial release.

5 Pin Configuration and Functions

**DCK Package
5-Pin SC70
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	1	I	Noninverting input
–IN	3	I	Inverting input
OUT	4	O	Output
V+	5	—	Positive (highest) supply
V–	2	—	Negative (lowest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted

			MIN	MAX	UNIT
Supply voltage, V_S				6	V
Signal input terminals	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	V
	Current		–10	10	mA
Output short-circuit			Continuous		mA
Operating temperature, T_A			–40	125	°C
Storage temperature, T_{stg}			–65	150	°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	2.25 (±1.125)	5.5 (±2.75)	V
T_A	Ambient operating temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC [1]		OPA375 DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	240.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	151.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64	°C/W
ψ_{JT}	Junction-to-top characterization parameter	34.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25 °C, V_S (total supply voltage) = (V+) – (V–) = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.15	±0.5	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±0.35		µV/°C
PSRR	Power supply rejection ratio	V_S = 2.25 V to 5.5 V, V_{CM} = (V–)	104	130		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–)		(V+) – 1.2	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.2 V	95	120		dB
INPUT BIAS CURRENT						
I_B	Input bias current			±10		pA
I_{OS}	Input offset current			±10		pA
NOISE						
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz		1.5		$µV_{p-p}$
e_n	Input voltage noise density	f = 10 kHz		3.7		nV/√Hz
		f = 1 kHz		5		nV/√Hz
i_n	Input current noise density	f = 1 kHz		26		fA/√Hz
INPUT CAPACITANCE						
C_{IN}	Differential			6		pF
	Common-mode			6		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V-) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ		125		dB
		(V-) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ	110	130		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = 1		10		MHz
	Phase margin	G = 1, R_L = 10 kΩ		55		Degrees
SR	Slew rate	G = 1		4.75		V/µs
t_S	Settling time	To 0.1%, 2-V step , G = 1		0.65		µs
		To 0.01%, 2-V step , G = 1		1.2		µs
	Overload recovery time	V_{IN} × Gain > V_S		0.2		µs
THD+N	Total harmonic distortion + noise	V_O = 1 V_{RMS}, V_{CM} = 2.5 V, G = 1, f = 1 kHz, R_L = 10 kΩ, V_S = 5.5 V		0.00035%		
OUTPUT						
V_O	Voltage output swing from supply rails	R_L = 10 kΩ		8	10	mV
Z_O	Open-loop output impedance	f = 10 MHz		160		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA		890		µA
		I_O = 0 mA, T_A = –40°C to +125°C			1.1	mA

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6.6 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

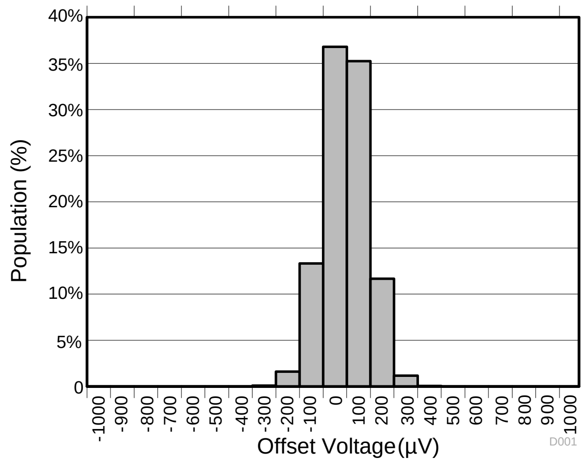


Figure 1. Offset Voltage Production Distribution

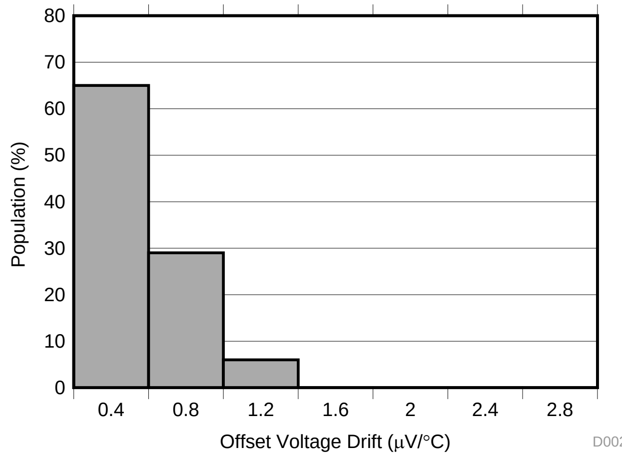


Figure 2. Offset Voltage Drift Distribution

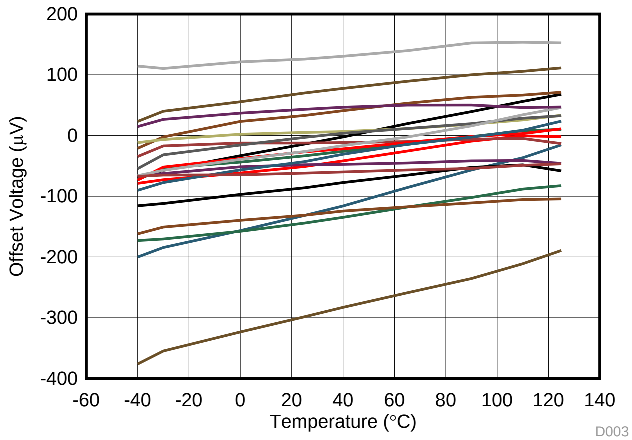


Figure 3. Offset Voltage vs Temperature

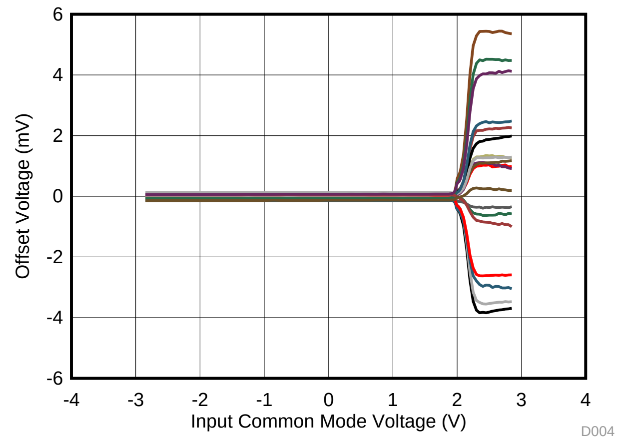


Figure 4. Offset Voltage vs Common-Mode Voltage

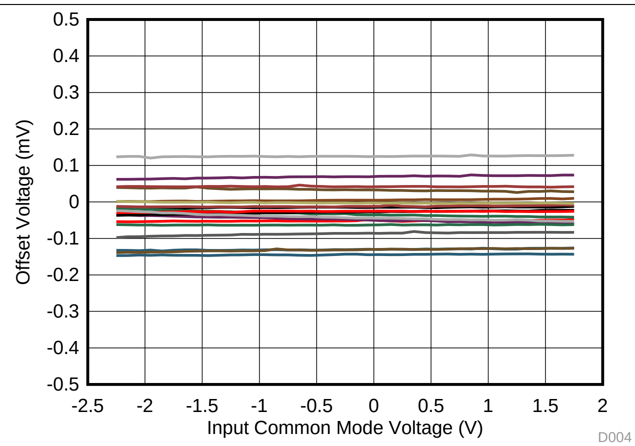


Figure 5. Offset Voltage vs Common-Mode Voltage

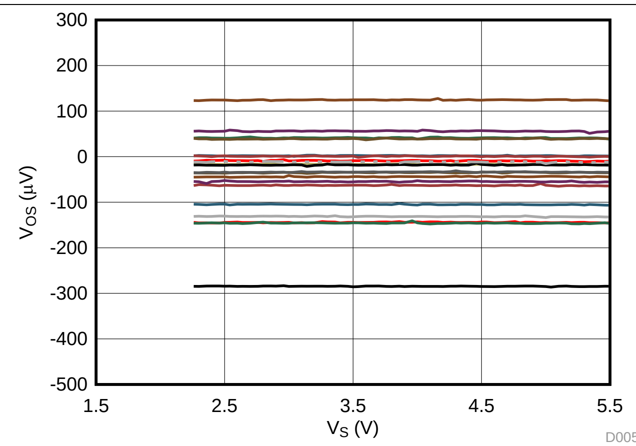


Figure 6. Offset Voltage vs Power Supply

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

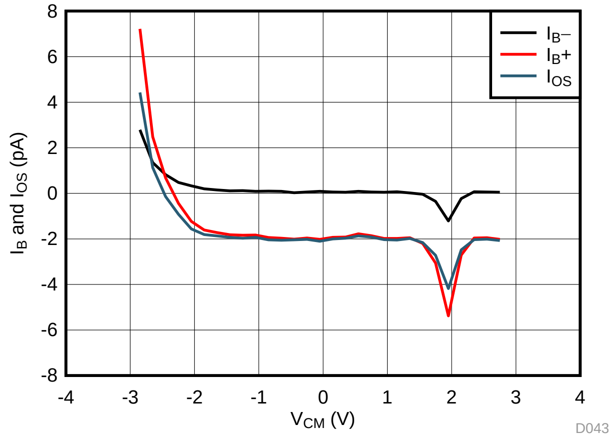


Figure 7. I_B and I_{OS} vs Common-Mode Voltage

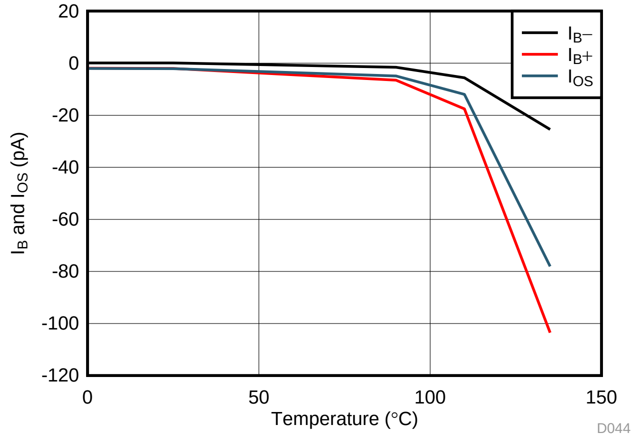
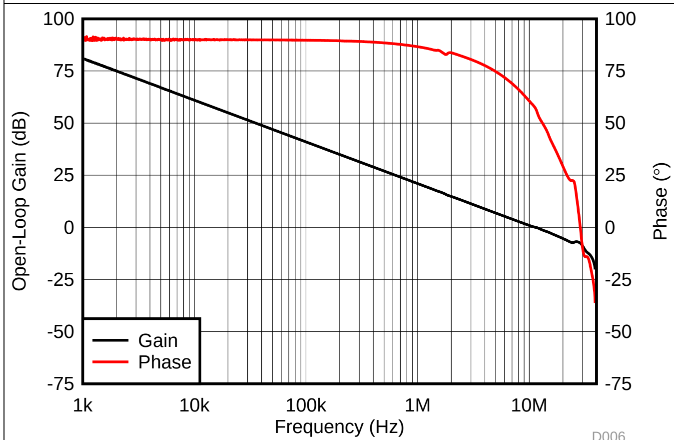


Figure 8. I_B and I_{OS} vs Temperature



C_L = 10 pF

Figure 9. Open-Loop Gain and Phase vs Frequency

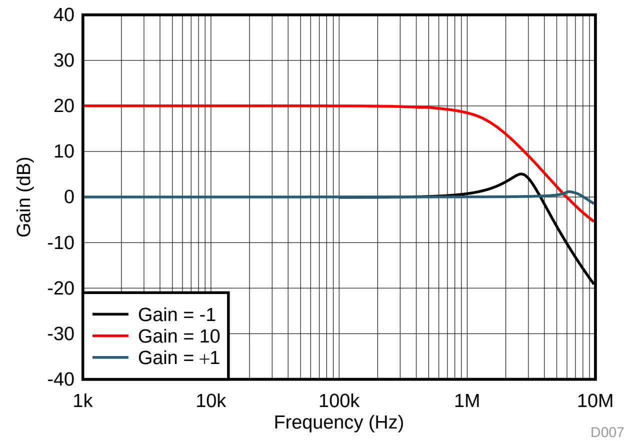


Figure 10. Closed-Loop Gain vs Frequency

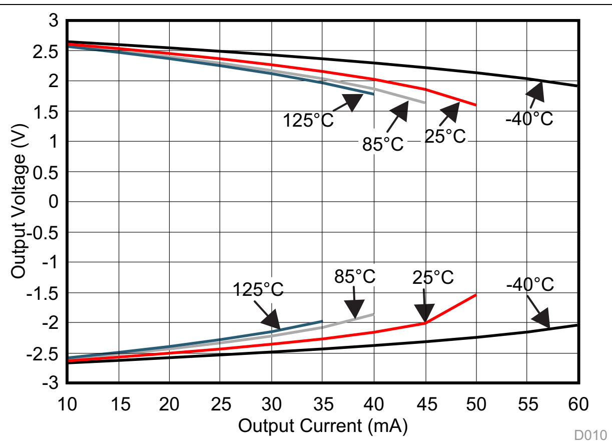


Figure 11. V_O vs I Sourcing and Sinking

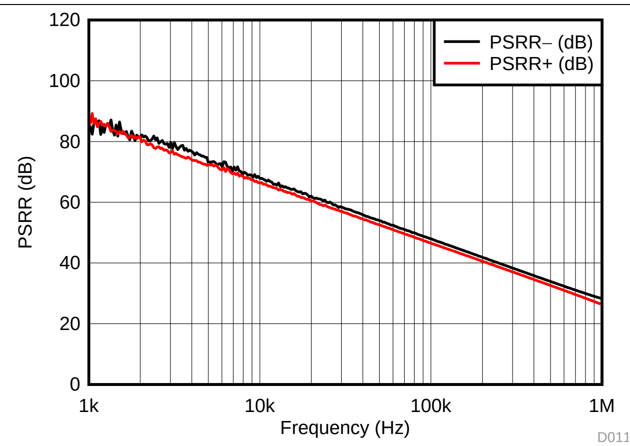


Figure 12. PSRR vs Frequency (Referred to Input)

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

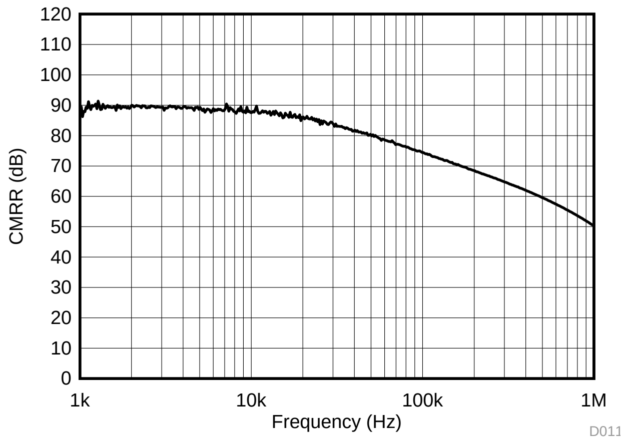
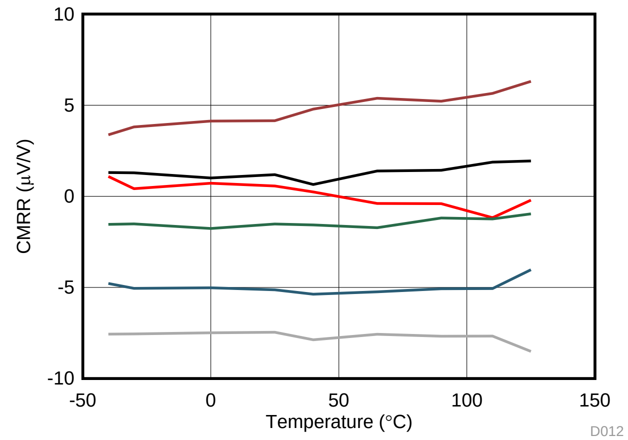


Figure 13. CMRR vs Frequency (Referred to Input)



V_S = 5.5 V T_A = –40°C to 125°C V_{CM} = 0 V to 4.3 V

Figure 14. CMRR vs Temperature

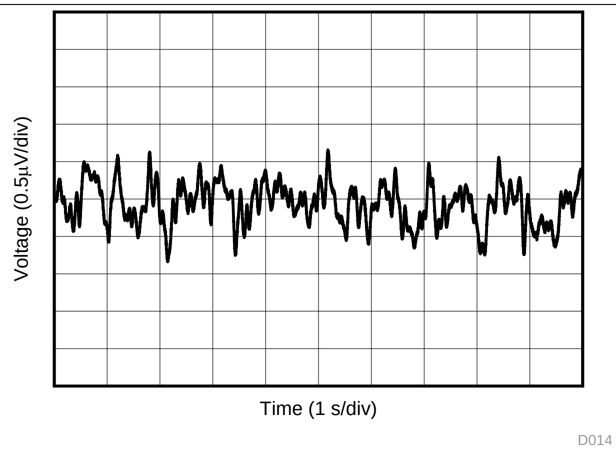


Figure 15. 0.1-Hz to 10-Hz Flicker Noise

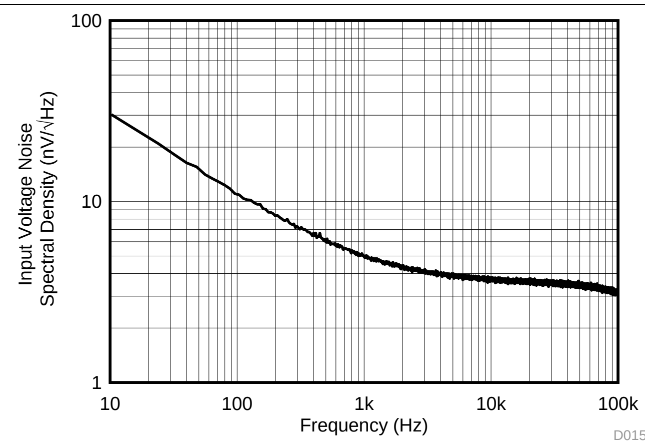
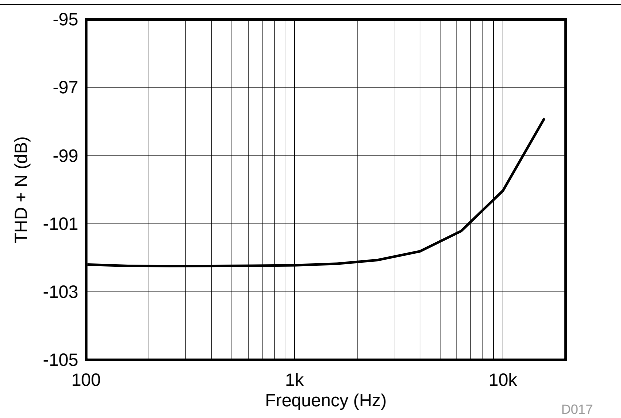
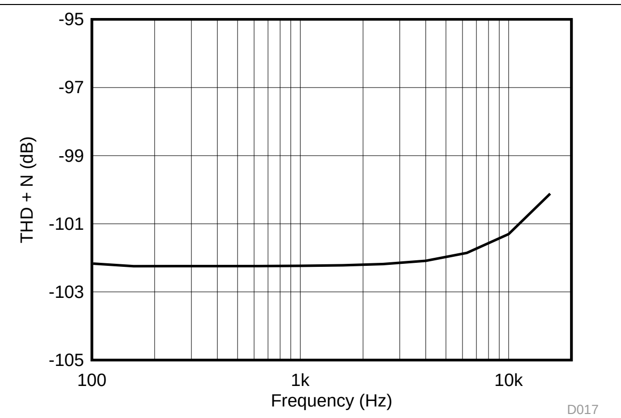


Figure 16. Input Voltage Noise Spectral Density vs Frequency



V_S = 5.5 V V_{ICM} = 2.5 V R_L = 2 kΩ
Gain = 1 BW = 80 kHz V_{OUT} = 0.5 Vrms

Figure 17. THD + N vs Frequency

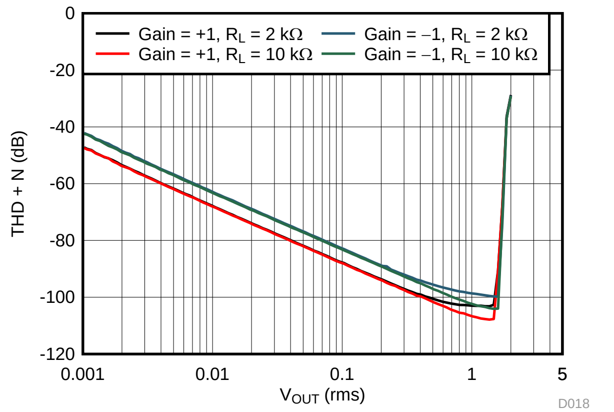


V_S = 5.5 V V_{ICM} = 2.5 V R_L = 10 kΩ
Gain = 1 BW = 80 kHz V_{OUT} = 0.5 Vrms

Figure 18. THD + N vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5.5 V V_{ICM} = 2.5 V BW = 80 kHz

V_{OUT} = 0.5 Vrms

Figure 19. THD + N vs Amplitude

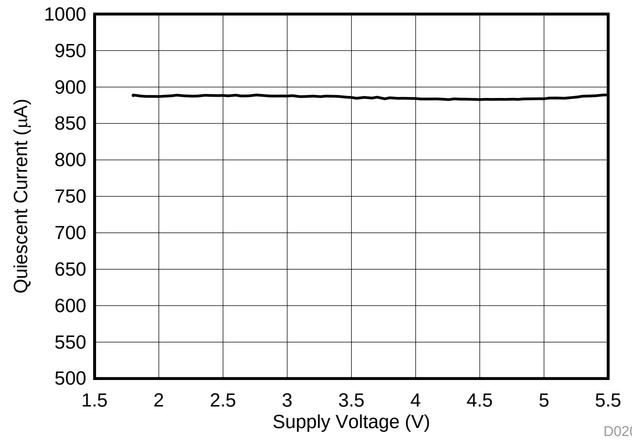


Figure 20. Quiescent Current vs Supply Voltage

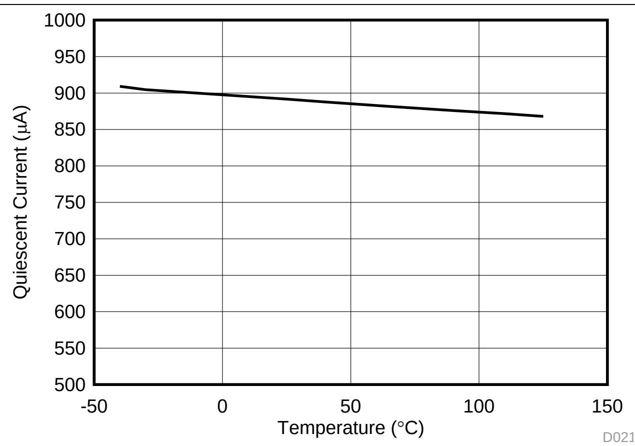
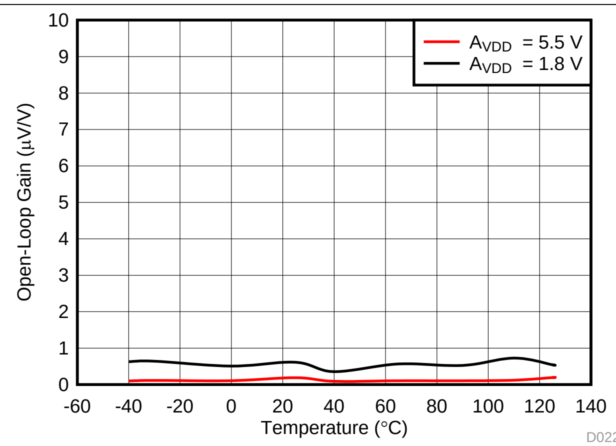


Figure 21. Quiescent Current vs Temperature



R_L = 2 kΩ

Figure 22. Open-Loop Gain vs Temperature

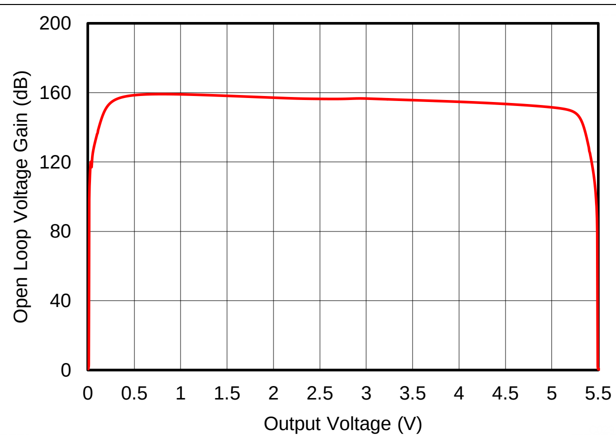
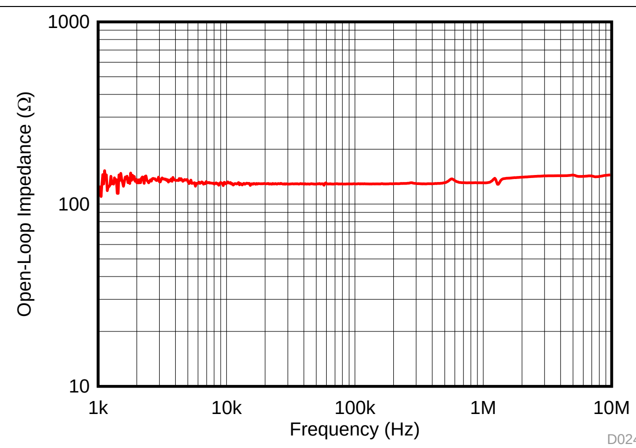


Figure 23. Open-Loop Gain vs Output Voltage

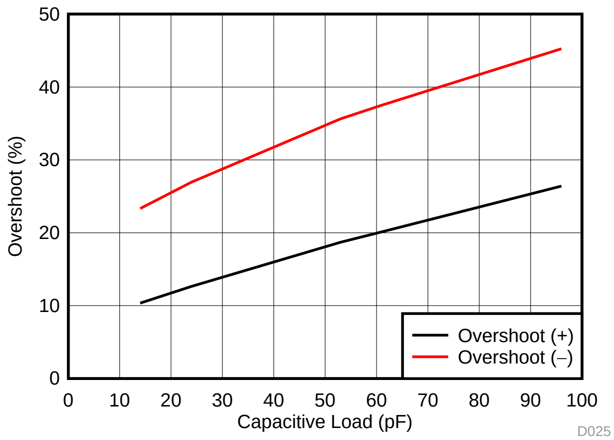


A_{VDD} = 5.5 V V_{ICM} = V_{OCM} = 2.75 V

Figure 24. Open-Loop Output Impedance vs Frequency

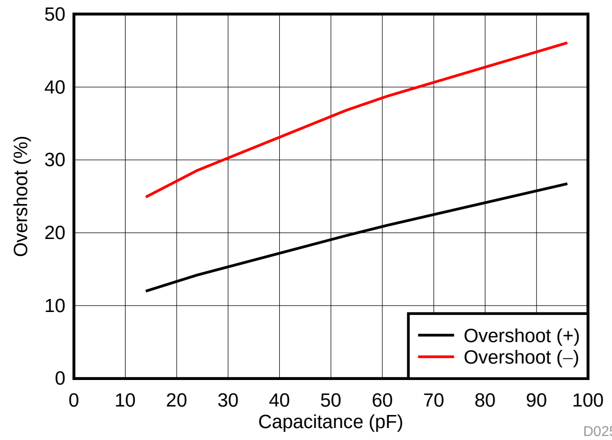
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



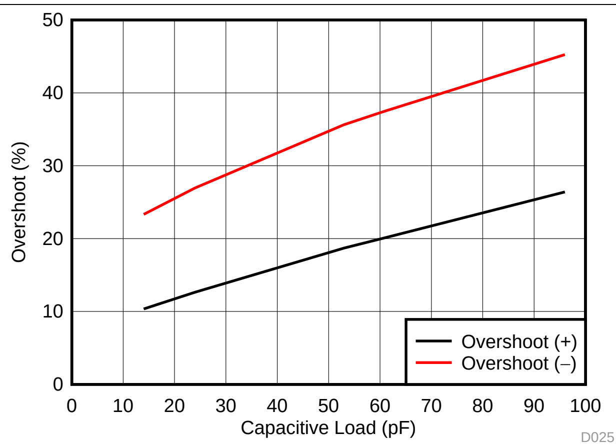
V_S = 5.5 V, V_{ICM} = 2.75 V, V_{OCM} = 2.75 V
G = 1, 100-mV output step

Figure 25. Small-Signal Overshoot vs Load Capacitance



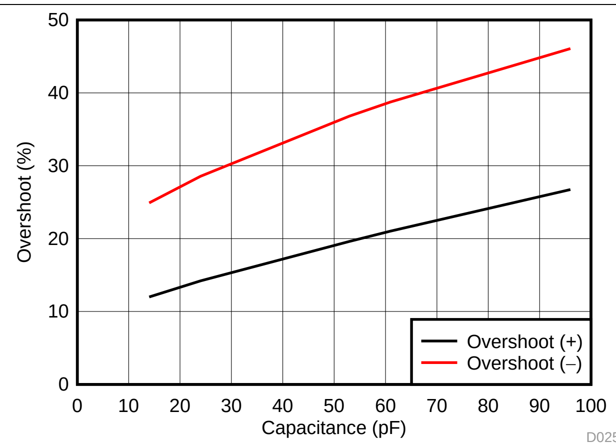
V_S = 1.8 V, V_{ICM} = 0.9 V, V_{OCM} = 0.9 V
G = 1, 100-mV output step

Figure 26. Small-Signal Overshoot vs Load Capacitance



V_S = 5.5 V, V_{ICM} = 2.75 V, V_{OCM} = 2.75 V
Gain = –1, 100-mV output step

Figure 27. Small-Signal Overshoot vs Load Capacitance



V_S = 1.8 V, V_{ICM} = 0.9 V, V_{OCM} = 0.9 V
Gain = –1, 100-mV output step

Figure 28. Small-Signal Overshoot vs Load Capacitance

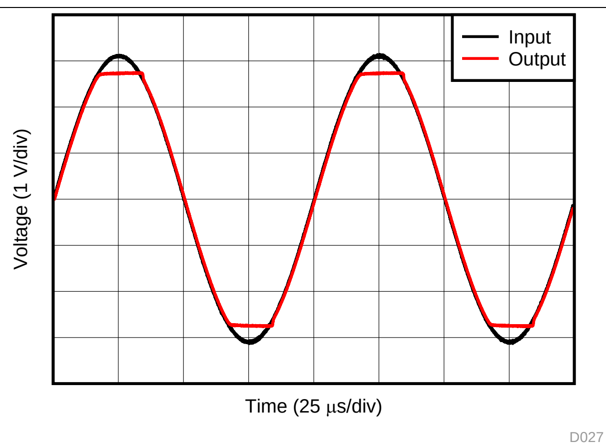


Figure 29. No Phase Reversal

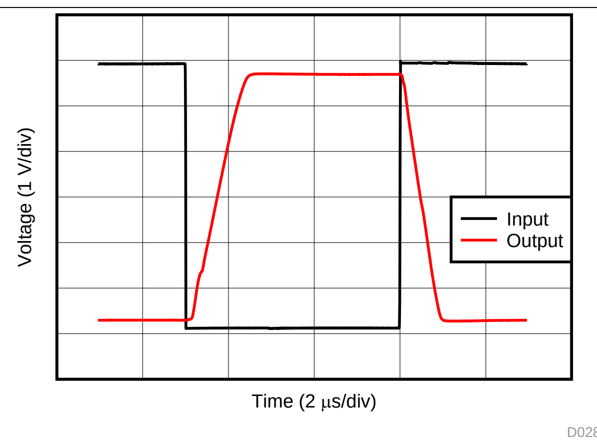
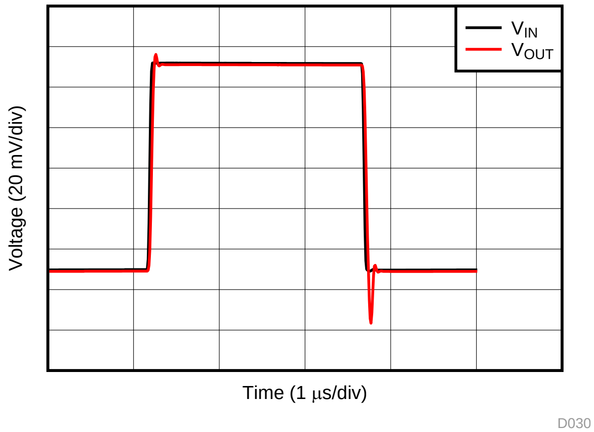


Figure 30. Overload Recovery

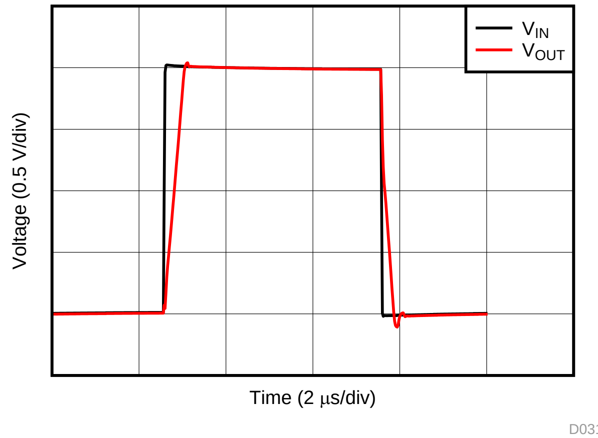
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



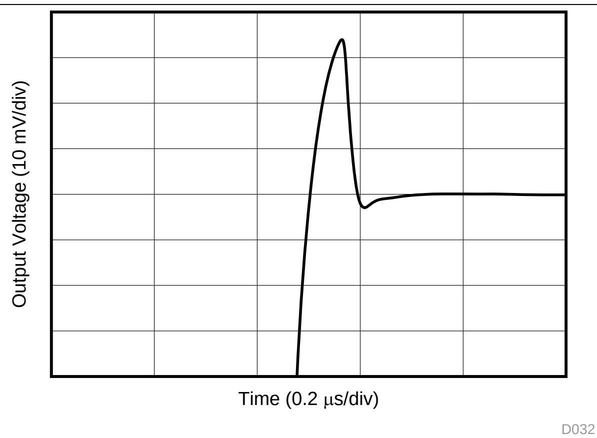
V_S = 1.8 V, V_{ICM} = 0.9 V, V_{OCM} = 0.9 V
C_L = 30 pF, Gain = 1, V_{IN} = 100 mVpp

Figure 31. Small-Signal Step Response



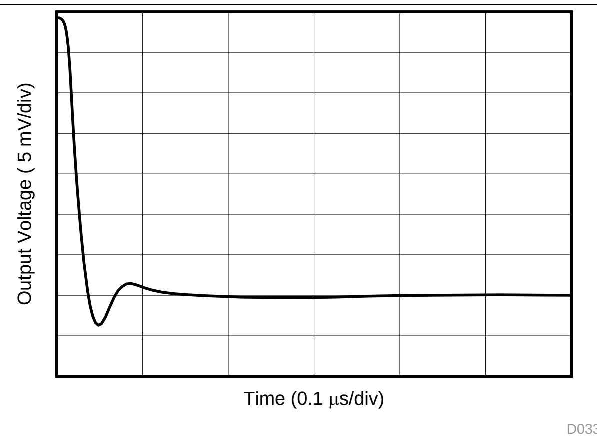
V_S = 5.5 V, V_{OCM} = 2.75 V, C_L = 10 pF
V_{ICM} = 2.75 V, Gain = 1, 2-V step

Figure 32. Large Signal Step Response



V_S = 5.5 V, V_{ICM} = 2.75 V, V_{OCM} = 2.75 V
C_L = 0, Gain = 1, 5-V step

Figure 33. Large Signal Settling Time (Positive)



V_S = 5.5 V, V_{ICM} = 2.75 V, V_{OCM} = 2.75 V
C_L = 0, Gain = 1, 5-V step

Figure 34. Large Signal Settling Time (Negative)

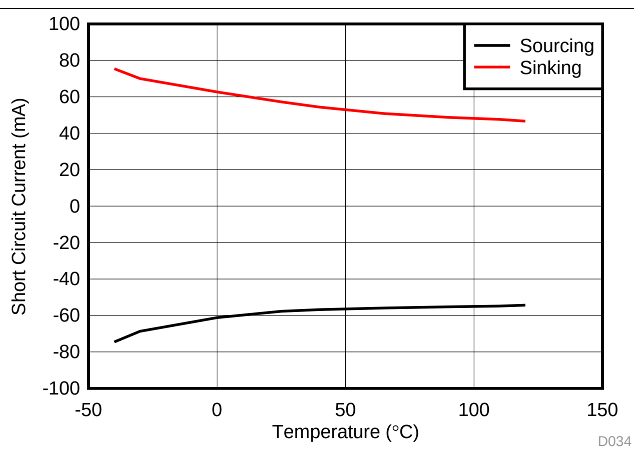
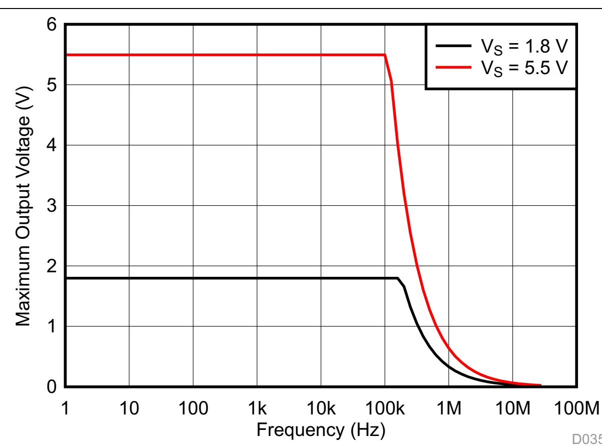


Figure 35. Short-Circuit Current vs Temperature



V_{ICM} = V_S / 2, V_{OCM} = V_S / 2, C_L = 10 pF
Gain = 1

Figure 36. Maximum Output Voltage vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

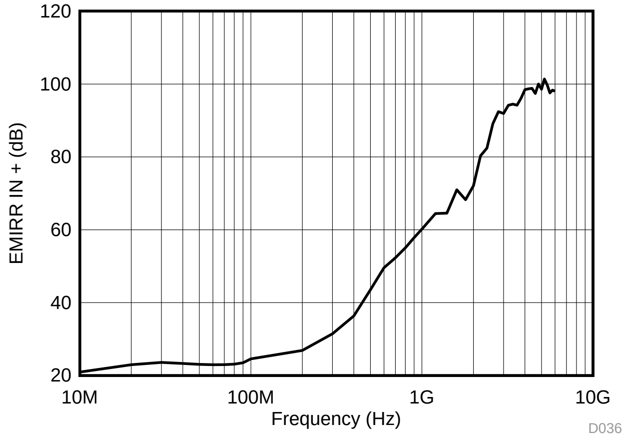
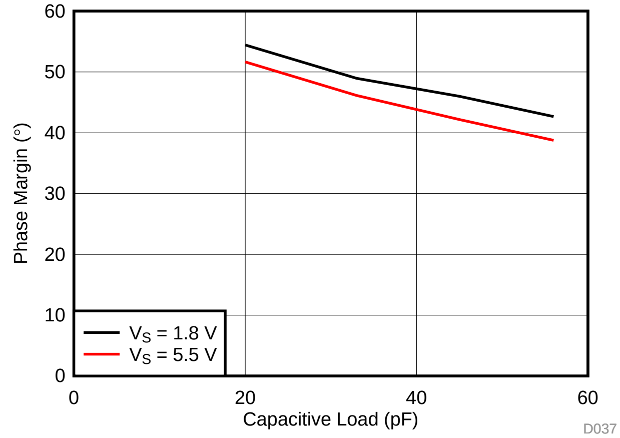


Figure 37. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



V_{ICM} = V_{OCM} = V_S / 2

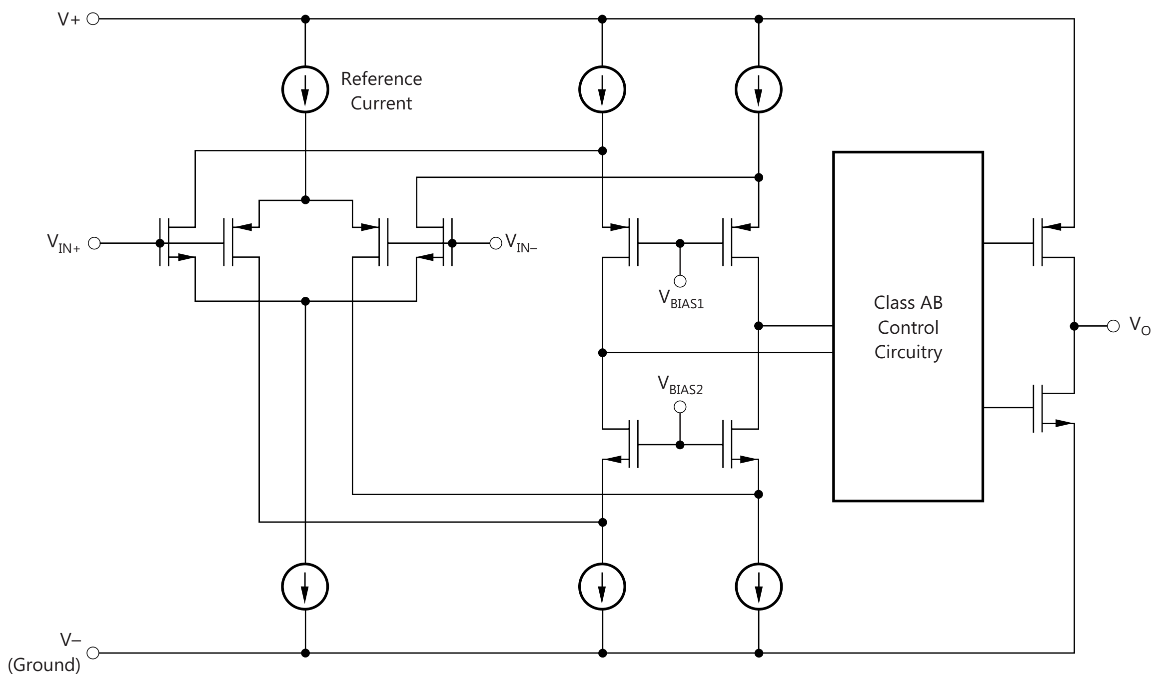
Figure 38. Phase Margin vs Capacitive Load

7 Detailed Description

7.1 Overview

The OPA375 is a ultra low-noise, rail-to-rail output operational amplifier. The device operates from a supply voltage of 2.25 V to 5.5 V, is unity-gain stable, and engineers can use this device for a wide range of general-purpose applications. The input common-mode voltage range includes the negative rail and allows the OPA375 op amp to be used in most single-supply applications. Rail-to-rail output swing significantly increases dynamic range, especially in low-supply applications, and as a result, the engineers can use the OPA375 device for audio applications and driving sampling analog-to-digital converters (ADCs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 THD+ Noise Performance

The OPA375 op amp has distortion characteristics. THD + noise is below 0.00035% (G = 1, V_O = 1 V_{RMS}. V_{CM} = 2.5 V, V_S = 5.5 V) throughout the audio frequency range, 20 Hz to 20 kHz, with a 10-kΩ load. The broadband noise of the OPA375 of 3.7 nV/√Hz is extremely low for a 10 MHz general-purpose amplifier.

7.3.2 Operating Voltage

The OPA375 op amp is fully specified and can operate from 2.25 V to 5.5 V. In addition, many specifications apply from –40°C to +125°C. Power-supply pins must be bypassed with 0.1-µF ceramic capacitors.

7.3.3 Rail-to-Rail Output

Designed as low-power, low-voltage op amps, the OPA375 delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within few mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails

Feature Description (continued)

7.3.4 Input and ESD Protection

The OPA375 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings*. Figure 39 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

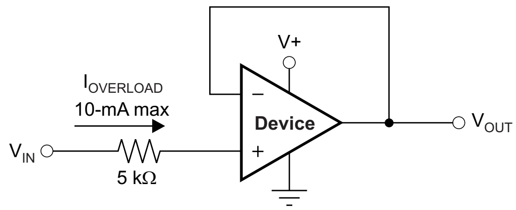


Figure 39. Input Current Protection

7.3.5 EMI Susceptibility and Input Filtering

Op amps vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the DC offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The OPA375 operational amplifier incorporates an internal input low-pass filter that reduces the response of the op amp to EMI. This filter provides common-mode and differential mode filtering.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. Detailed information can also be found in *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

7.4 Device Functional Modes

The OPA375 device has a single functional mode. This device is powered on as long as the power-supply voltage is between 2.25 V (±1.125 V) and 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA375 device features 10-MHz bandwidth and 4.75-V/µs slew rate with 890-µA of supply current per channel, providing good AC performance at low-power consumption. DC applications are well served with a low input noise voltage of 3.7 nV / √Hz at 10 kHz, low input bias current, and a typical input offset voltage of 0.15 mV.

8.2 Single-Supply Electret Microphone Pre-amplifier With Speech Filter

Electret microphones are commonly used in portable electronics because of the small size, low cost, and relatively good signal-to-noise ratio (SNR). The small package size, low operating voltage and AC performance of the OPA375 make the device a viable option for pre-amplifier circuits for electret microphones. The circuit shown in Figure 40 is a single-supply pre-amplifier circuit for electret microphones.

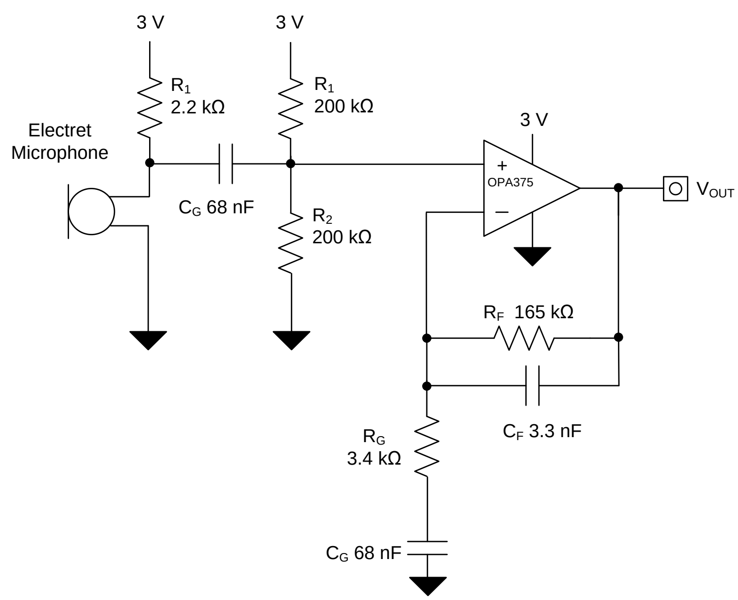


Figure 40. Microphone Pre-Amplifier

8.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 3 V
- Input voltage: 7.93 mV_{RMS} (0.63 Pa with a –38 dB SPL microphone)
- Output: 1 V_{RMS}
- Bandwidth: 300 Hz to 3 kHz

8.2.2 Detailed Design Procedure

The transfer function defining the relationship between V_{OUT} and the AC input signal is shown in Equation 1:

Single-Supply Electret Microphone Pre-amplifier With Speech Filter (continued)

$$V_{OUT} = V_{IN\_AC} \times \left(1 + \frac{R_F}{R_G}\right) \tag{1}$$

The required gain can be calculated based on the expected input signal level and desired output level as shown in Equation 2

$$G_{OPA} = \frac{V_{OUT}}{V_{IN\_AC}} = \frac{1V_{RMS}}{7.93mV_{RMS}} = 126\frac{V}{V} \tag{2}$$

Select a standard 10-kΩ feedback resistor and calculate R_G from Equation 3.

$$R_G = \frac{R_F}{G_{OPA} - 1} = \frac{10k\Omega}{126\frac{V}{V} - 1} = 80\Omega \rightarrow 78.7\Omega \text{ (closest standard value)} \tag{3}$$

To minimize the attenuation in the desired passband from 300 Hz to 3 kHz set the upper (f_H) and lower (f_L) cutoff frequencies outside of the desired bandwidth as:

$$f_L = 200\text{ Hz} \tag{4}$$

and

$$f_H = 5\text{ kHz} \tag{5}$$

Select C_G to set the f_L cutoff frequency using Equation 6:

$$C_G = \frac{1}{2 \times \pi \times R_G \times f_L} = \frac{1}{2 \times \pi \times 78.7\Omega \times 200Hz} = 10.11\mu F \rightarrow 10\mu F \tag{6}$$

Select C_F to set the f_H cutoff frequency using Equation 7

$$C_F = \frac{1}{2 \times \pi \times R_F \times f_H} = \frac{1}{2 \times \pi \times 10k\Omega \times 5kHz} = 3.18nF \rightarrow 3.3nF \text{ (Standard Value)} \tag{7}$$

The input signal cutoff frequency must be set low enough such that low-frequency sound waves still pass through. Therefore select C_{IN} to achieve a 30-Hz cutoff frequency (f_{IN}) using Equation 8.

$$C_{IN} = \frac{1}{2 \times \pi \times (R_1 \| R_2) \times f_{IN}} = \frac{1}{2 \times \pi \times 100k\Omega \times 30Hz} = 53nF \rightarrow 68nF \text{ (Standard Value)} \tag{8}$$

The measured transfer function for the microphone preamplifier circuit is shown in Figure 41 and The measured THD+N performance of the microphone preamplifier circuit is shown in Figure 42.

Single-Supply Electret Microphone Pre-amplifier With Speech Filter (continued)

8.2.3 Application Curves

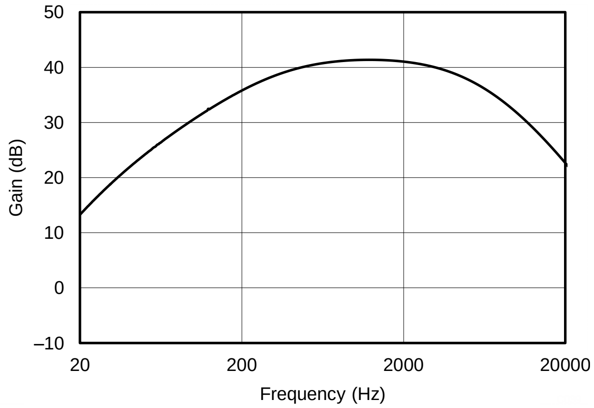


Figure 41. Gain vs Frequency

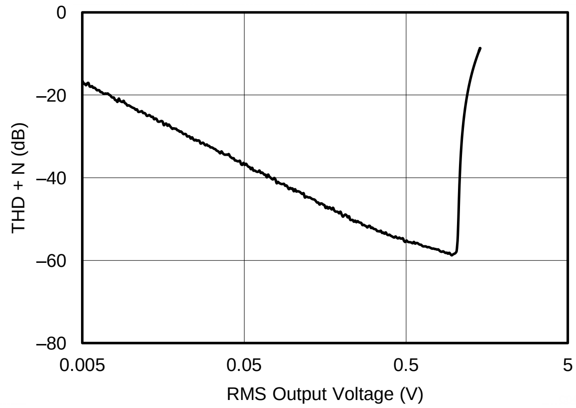


Figure 42. THD + N vs RMS Output Voltage

9 Power Supply Recommendations

The OPA375 device is specified for operation from 2.25 V to 5.5 V (±1.125 V to ±2.75 V); many specifications apply from –40°C to +125°C. Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in Figure 43.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

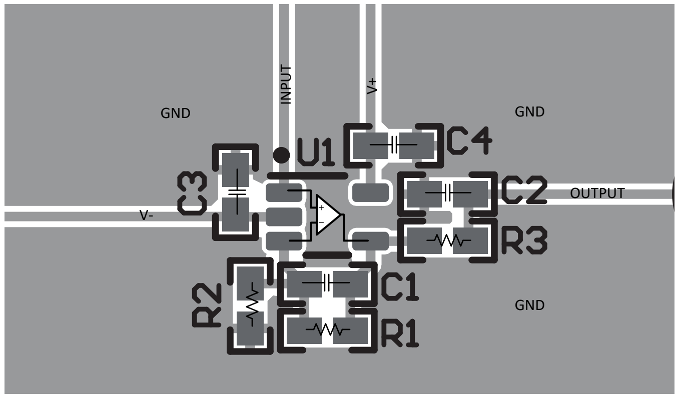


Figure 43. Operational Amplifier Board Layout for Noninverting Configuration

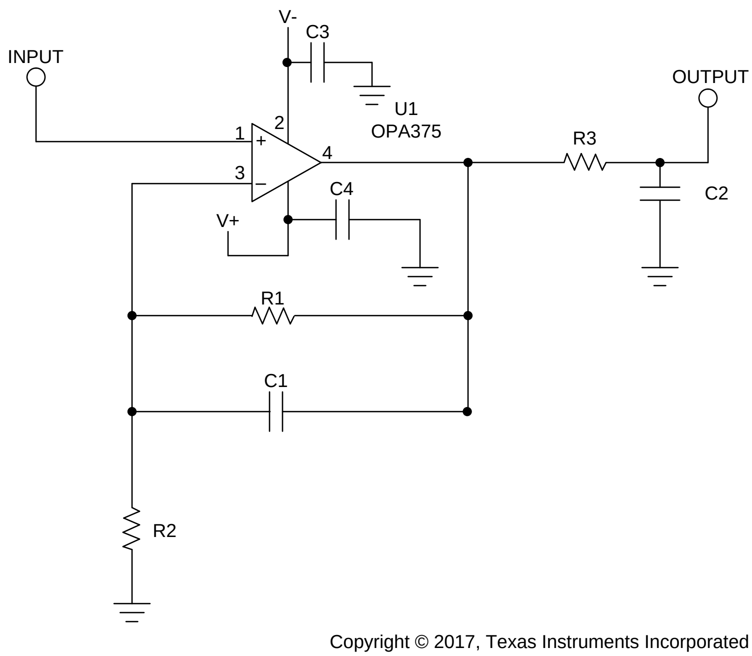


Figure 44. Layout Example Schematic

11 Device and Documentation Support

11.1 Device Support

11.1.1 DFN Package

NOTE
The exposed leadframe die pad on the bottom of the DFN package should be connected to the most negative potential (V–).

11.1.2 Documentation Support

11.1.2.1 Related Documentation

For related documentation see the following:

- *QFN/SON PCB Attachment*
- *Quad Flatpack No-Lead Logic Packages*
- *Circuit Board Layout Techniques*
- *EMI Rejection Ratio of Operational Amplifiers*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA375IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19W	Samples
OPA375IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

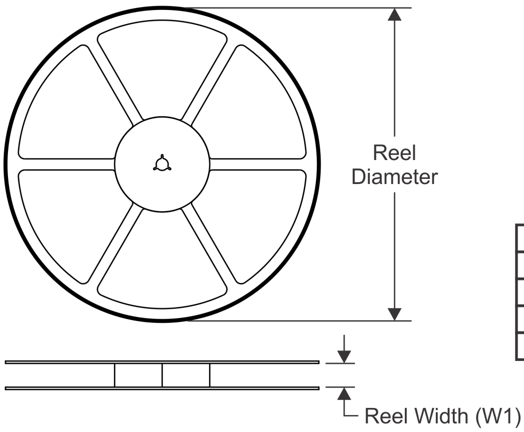
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

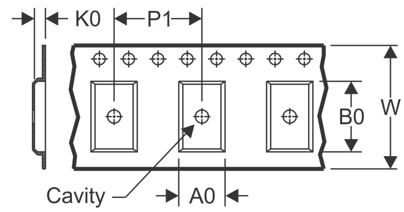
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

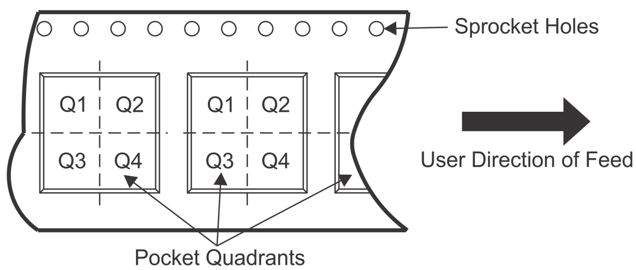


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

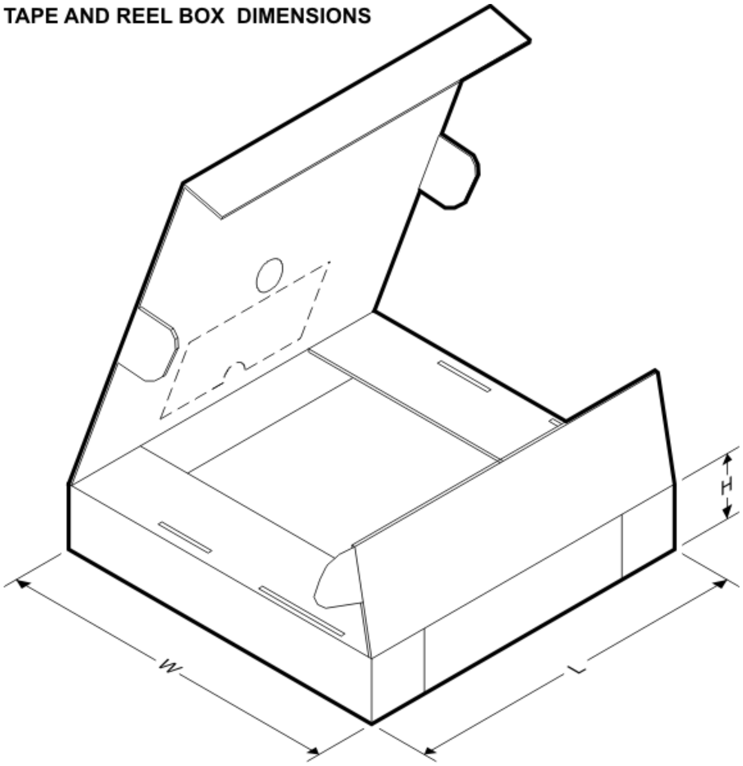
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA375IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA375IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

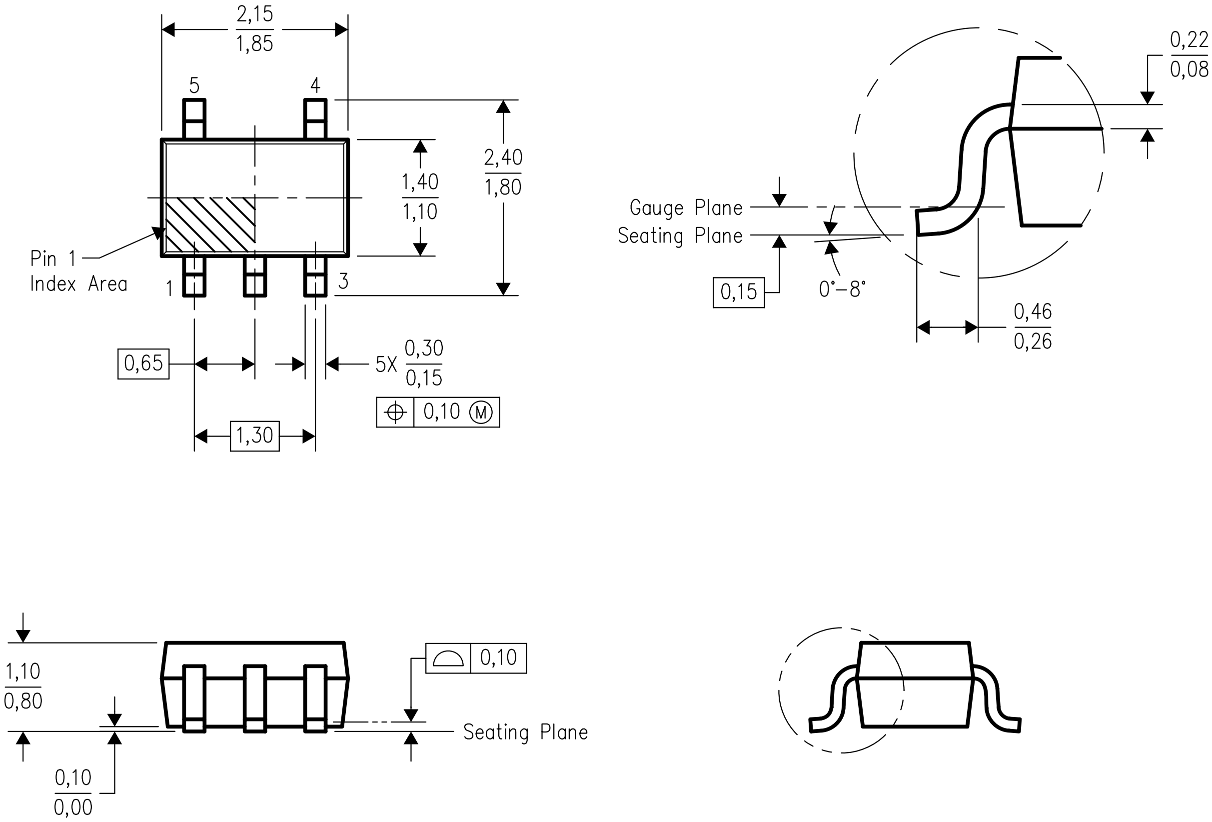
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA375IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
OPA375IDCKT	SC70	DCK	5	250	190.0	190.0	30.0

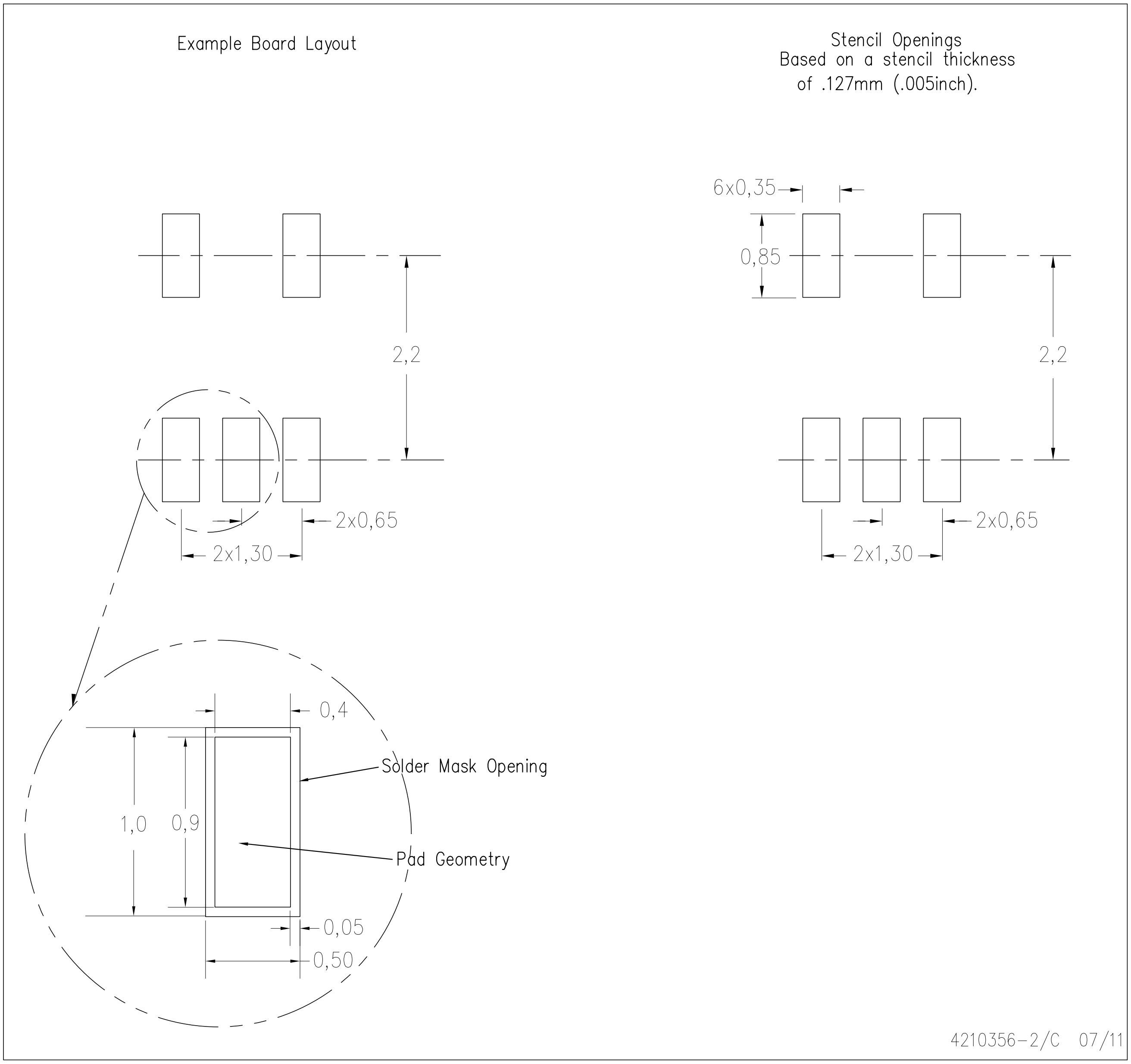
DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.