

## SYNCHRONOUS-BUCK MOSFET DRIVERS WITH DRIVE REGULATOR

### FEATURES

- Integrated Drive Regulator (4 V to 14 V)
- Adjustable/Adaptive Dead-Time Control
- 4-A Peak current at VDRV of 14 V
- 10-V to 15-V Supply Voltage Range
- TTL-Compatible Inputs
- Internal Schottky Diode Reduces Part Count
- Synchronous or Nonsynchronous Operation

- Inverting and Noninverting Options
- TSSOP PowerPad™ Package for Excellent Thermal Performance

### APPLICATIONS

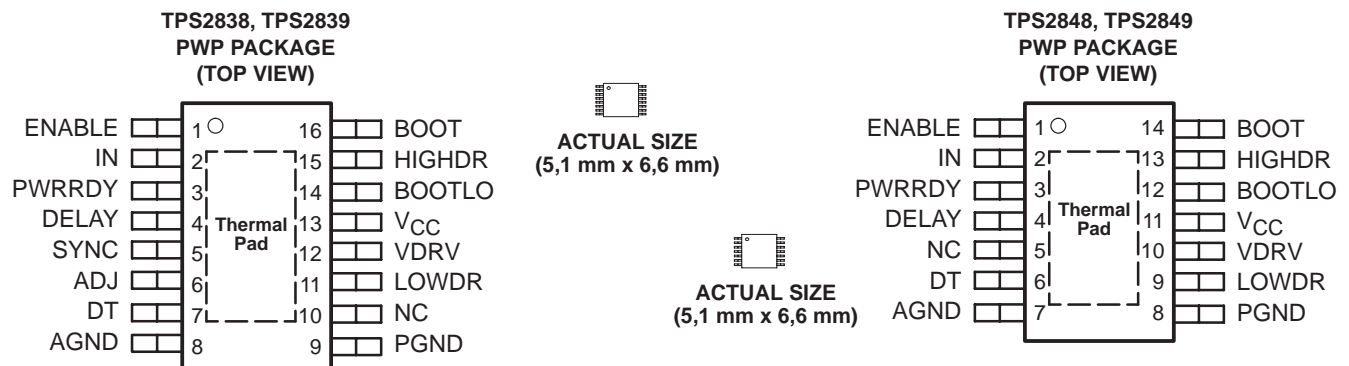
- Single or Multiphase Synchronous-Buck Power Supplies
- High-Current DC/DC Power Modules

### DESCRIPTION

The TPS2838/39/48/49 devices are MOSFET drivers designed for high-performance synchronous power supplies. The drivers can source and sink up to 4-A peak current at a 14-V drive voltage. These are ideal devices to use with power supply controllers that do not have on-chip drivers. The low-side driver is capable of driving loads of 3.3 nF in 10-ns rise/fall times and has 40-ns propagation delays at room temperature.

The MOSFET drivers have an integrated 150-mA regulator, so the gate drive voltage can be optimized for specific MOSFETs. The TPS2848 and TPS2849 have a fixed 8-V drive regulator, while the TPS2838/39 allow the drive regulator to be adjusted from 4 V to 14 V by selection of two external resistors.

The devices feature VDRV to PGND shoot-through protection with adaptive/adjustable deadtime control. The deadtime, for turning on the high-side FET from LOWDR transitioning low, is adjustable with an external capacitor on the DELAY pin. This allows compensation for the effect the gate resistor has on the synchronous FET turn off. The adaptive deadtime prevents the turning on of the low-side FET until the voltage on the BOOTLO pin falls below a threshold after the high-side FET stops conducting. The high-side drive can be configured as a ground referenced driver or a floating bootstrap driver. The internal Schottky diode minimizes the size and number of external components needed for the bootstrap driver circuit. Only one external ceramic capacitor is required to configure the bootstrap driver.



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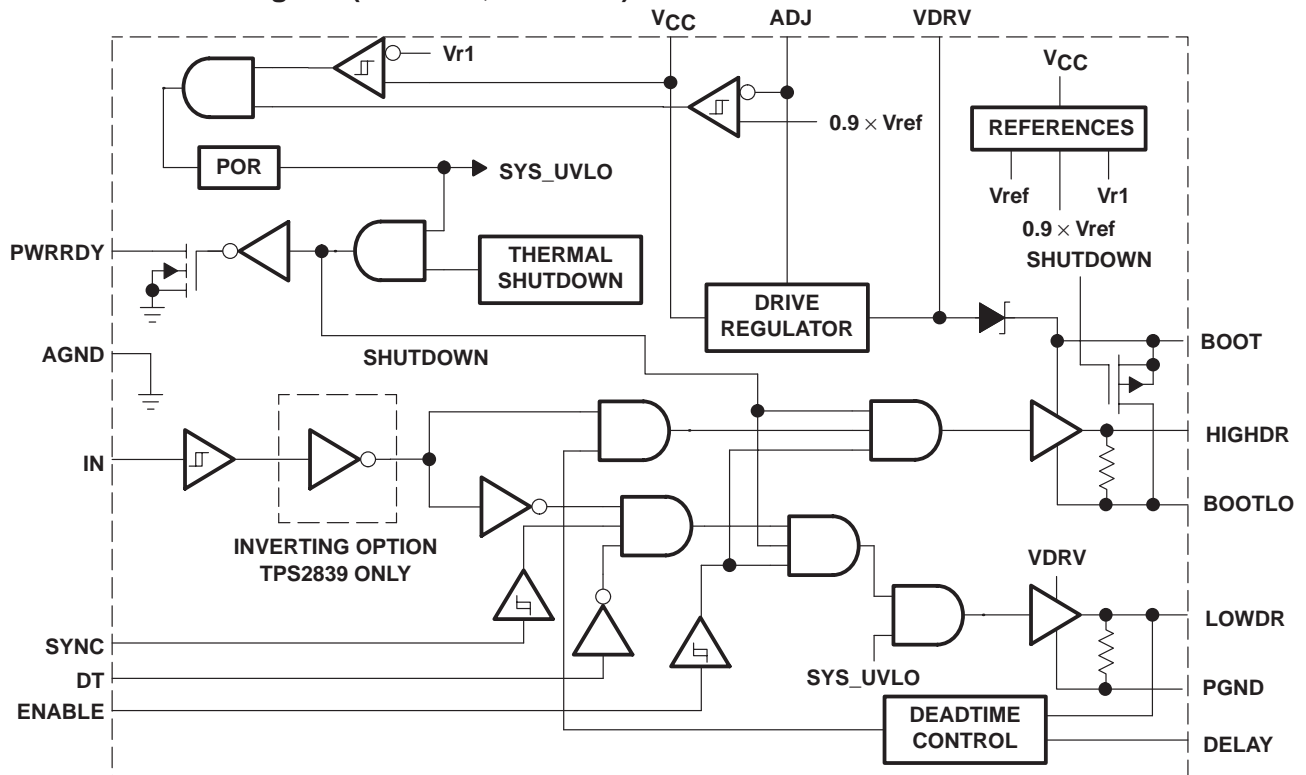
**description (continued)**

The SYNC pin can be used regardless of load to disable the synchronous FET driver and operate the power supply nonsynchronously.

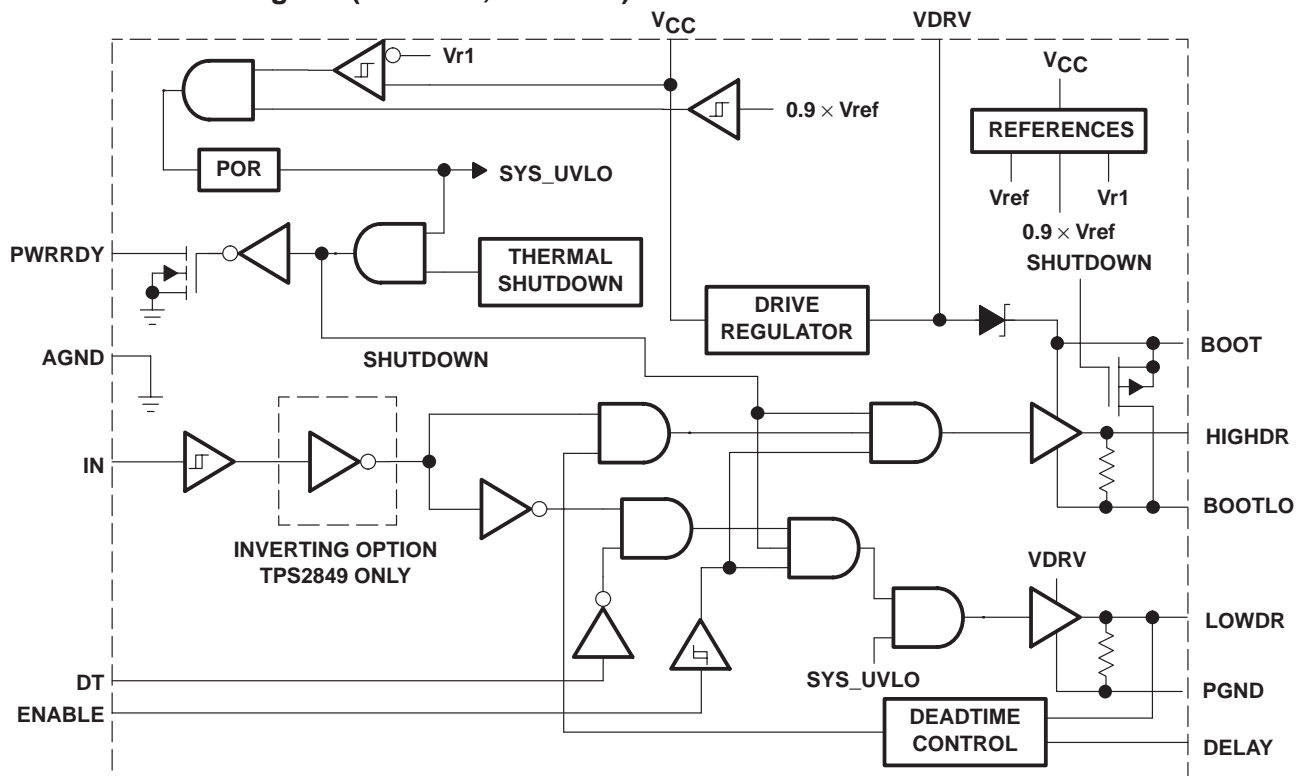
A power ready/undervoltage lockout function outputs the status of the  $V_{CC}$ -pin voltage and driver regulator output on the open-drain PWRRDY pin. This feature can be used to enable a controller's output once the  $V_{CC}$  voltage reaches the threshold and the regulator output is stable. This function ensures both FET drivers are off when the  $V_{CC}$  voltage is below the voltage threshold.

The TPS2838/39/48/49 devices are offered in the thermally enhanced 14-pin and 16-pin PowerPAD TSSOP package. The PowerPAD package features an exposed leadframe on the bottom that can be soldered to the printed-circuit board to improve thermal efficiency. The TPS2838/48 are noninverting control logic while the TPS2839/49 drivers are inverting control logic.

functional block diagram (TPS2838, TPS2839)



functional block diagram (TPS2848, TPS2849)



**Terminal Functions**

TERMINAL			DESCRIPTION
NAME	NO.		
	TPS283x	TPS284x	
ADJ	6	—	Adjust. The adjust pin is the feedback pin for the drive regulator (TPS283X only)
AGND	8	7	Analog ground
BOOT	16	14	Bootstrap. A capacitor is connected between the BOOT and BOOTLO pins to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1 $\mu$ F and 1 $\mu$ F.
BOOTLO	14	12	Boot low. This pin connects to the junction of the high-side and low-side MOSFETs.
DELAY	4	4	Delay. Connecting a capacitor between this pin and ground adjusts the deadtime for high-side driver
DT	7	6	Deadtime control. Connect DT to the junction of the high-side and low-side MOSFETs
ENABLE	1	1	Enable. If ENABLE is low, both drivers are off.
HIGHDR	15	13	High drive. This pin is the output drive for the high-side power MOSFET.
IN	2	2	Input. This pin is the input signal to the MOSFET drivers.
LOWDR	11	9	Low drive. This pin is the output drive for the low-side power MOSFET.
NC	10	5	No internal connection
PGND	9	8	Power ground. This pin is connected to the FET power ground.
PWRRDY	3	3	Power ready. This open-drain pin indicates a power good for VDRV and $V_{CC}$ .
SYNC	5	—	Synchronous rectifier enable. If SYNC is low, the low-side driver is always off; if SYNC is high, the low-side driver provides gate drive to the low-side MOSFET.
$V_{CC}$	13	11	Input power supply. It is recommended that a capacitor (minimum 1 $\mu$ F) be connected from $V_{CC}$ to PGND. Note that $V_{CC}$ must be 2 V higher than VDRV.
VDRV	12	10	Drive regulator output voltage. It is recommended that a capacitor (minimum 1 $\mu$ F) be connected from VDRV to PGND. Note that $V_{CC}$ must be 2 V higher than VDRV.

**detailed description**

**low-side driver**

The low-side driver is designed to drive low  $r_{DS(on)}$  N-channel MOSFETs. The current rating of the driver is 4 A, source and sink.

**high-side driver**

The high-side driver is designed to drive low  $r_{DS(on)}$  N-channel MOSFETs. The current rating of the driver is 4 A minimum, source and sink. The high-side driver can be configured as a GND-reference driver or as a floating-bootstrap driver. The internal bootstrap diode is a Schottky, for improved drive efficiency. The maximum voltage that can be applied from BOOT to ground is 30 V.

**dead-time (DT) control**

Dead-time control prevents shoot-through current from flowing through the main power FETs during switching transitions by controlling the turnon times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is low, and the low-side driver is not allowed to turn on until the voltage at the junction of the power FETs (BOOTLO) is low. The TTL-compatible DT terminal connects to the junction of the power FETs.

**ENABLE**

The ENABLE terminal enables the drivers. When enable is low, the output drivers are low. ENABLE is a TTL-compatible digital terminal.

**detailed description (continued)**

**IN**

The IN terminal is a TTL-compatible digital terminal that is the input control signal for the drivers. The TPS2838/48 have noninverting inputs; the TPS2839/49 have inverting inputs. On the TPS2838 and TPS2848, a high on IN results in a high on HIGHDR. On the TPS2839 and TPS2849, a high on IN results in a low on HIGHDR.

**SYNC (TPS283x only)**

The SYNC terminal controls whether the drivers operate in synchronous or nonsynchronous mode. In synchronous mode, the low-side FET is operated as a synchronous rectifier. In nonsynchronous mode, the low-side FET is always off. SYNC is a TTL-compatible digital terminal.

**PWRRDY**

Depicts the status of the  $V_{CC}$  pin voltage and the driver regulator output on the open-drain PWRRDY pin.

**DELAY**

Adjustable high-side turnon delay from from when the low-side FET is turned off.

**ADJ (TPS283x only)**

Input for adjusting the driver regulator output. See the *application information* section for the adjustment formula.

**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ (see Note 1)	–0.3 V to 16 V
Input voltage range: ADJ	–0.3 V to 7 V
BOOT to PGND (high-side driver ON)	–0.3 V to 30 V
BOOTLO to PGND	–0.3 V to 16 V
BOOT to BOOTLO	–0.3 V to 16 V
ENABLE, IN, and SYNC	–0.3 V to 16 V
VDRV, PWRRDY, and DELAY	–0.3 V to 16 V
DT	–0.3 V to 16 V
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$	–40°C to 125°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to PGND.

# TPS2838, TPS2839 TPS2848, TPS2849

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DISSIPATION RATING TABLE

PACKAGE	T <sub>A</sub> ≤ 25°C	DERATING FACTOR	T <sub>A</sub> = 70°C	T <sub>A</sub> = 85°C
14-pin PWP with solder†	2668	26.68 mW/°C	1467	1067
14-pin PWP without solder†	1024	10.24 mW/°C	563	409
16-pin PWP with solder†	2739	27.39 mW/°C	1506	1095
16-pin PWP without solder†	1108	11.08 mW/°C	609	443

JUNCTION-CASE THERMAL RESISTANCE TABLE

14-pin PWP	Junction-case thermal resistance	2.07 °C/W
16-pin PWP	Junction-case thermal resistance	2.07 °C/W

† Test Board Conditions:

1. Thickness: 0.062"
2. 3" × 3" (for packages < 27 mm long)
3. 4" × 4" (for packages > 27 mm long)
4. 2-oz copper traces located on the top of the board (0,071 mm thick)
5. Copper areas located on the top and bottom of the PCB for soldering
6. Power and ground planes, 1-oz copper (0,036 mm thick)
7. Thermal vias, 0,33 mm diameter, 1,5 mm pitch
8. Thermal isolation of power plane

For more information, refer to TI technical brief literature number SLMA002.

## recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>	10		15	V
Input voltage, V <sub>I</sub>   BOOT to PGND	10		29	V

electrical characteristics over recommended operating virtual junction temperature range,  
V<sub>CC</sub> = 12 V, ENABLE = High, C<sub>L</sub> = 3.3 nF (unless otherwise noted)

## supply current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>CC</sub> Quiescent current	V(ENABLE) = Low, V <sub>CC</sub> = 13 V			425	μA
	V(ENABLE) = High, V <sub>CC</sub> = 13 V			1	mA

NOTE 2: Ensured by design, not production tested.

electrical characteristics over recommended operating virtual junction temperature range,  
V<sub>CC</sub> = 12 V, ENABLE = High, C<sub>L</sub> = 3.3 nF (unless otherwise noted) (continued)

dead-time control

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IH</sub> (LOWDR) LOWDR high-level input voltage	Over full VDRV range See Note 2	50			%VDRV
V <sub>IL</sub> (LOWDR) LOWDR low-level input voltage	Over full VDRV range See Note 2			1	V
V <sub>IH</sub> (DT) DT high-level input voltage	Over full V <sub>CC</sub> range	2			V
V <sub>IL</sub> (DT) DT low-level input voltage	Over full V <sub>CC</sub> range			1	V
Deadtime delay	V(VDRV) = 4 V to 14 V See Note 2	0.5	1	1.5	ns/pF
Driver nonoverlap time (DT to LOWDR)	V(VDRV) = 4.5 V, T <sub>J</sub> = 25°C, See Note 2	30		150	ns
	V(VDRV) = 14.5 V, T <sub>J</sub> = 25°C, See Note 2	30		100	ns
Driver nonoverlap time (LOWDR to HIGHDR)	V(VDRV) = 4.5 V, C <sub>L</sub> (Delay) = 50 pF T <sub>J</sub> = 25°C, See Note 2	75		180	ns
	V(VDRV) = 14.5 V, C <sub>L</sub> (Delay) = 50 pF T <sub>J</sub> = 25°C, See Note 2	58		125	
Driver nonoverlap time (LOWDR to HIGHDR)	V(VDRV) = 4.5 V, C <sub>L</sub> (Delay) = 0 pF T <sub>J</sub> = 25°C, See Note 2	50		125	ns
	V(VDRV) = 14.5 V, C <sub>L</sub> (Delay) = 0 pF T <sub>J</sub> = 25°C, See Note 2	30		100	

NOTE 2: Ensured by design, not production tested.

high-side driver

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output current	V(BOOT) – V(BOOTLO) = 4 V, See Note 2	V(HIGHDR) = 0.5 V (src)	1	1.3	A
		V(HIGHDR) = 4 V (sink)	2	2.4	
	V(BOOT) – V(BOOTLO) = 8 V, See Note 2	V(HIGHDR) = 0.5 V (src)	2	2.4	
		V(HIGHDR) = 8 V (sink)	2	3.3	
	V(BOOT) – V(BOOTLO) = 14 V, See Note 2	V(HIGHDR) = 0.5 V (src)	2	3.9	
		V(HIGHDR) = 14 V (sink)	2	4.4	
r <sub>o</sub> Output resistance	V(BOOT) – V(BOOTLO) = 4.5 V T <sub>J</sub> = 25°C	V(HIGHDR) = 4 V (src)		45	Ω
		V(HIGHDR) = 0.5 V (sink)		6	
	V(BOOT) – V(BOOTLO) = 7.5 V, T <sub>J</sub> = 25°C	V(HIGHDR) = 7 V (src)		26	
		V(HIGHDR) = 0.5 V (sink)		5	
	V(BOOT) – V(BOOTLO) = 11.5 V, T <sub>J</sub> = 25°C	V(HIGHDR) = 11 V (src)		20	
		V(HIGHDR) = 0.5 V (sink)		4	
HIGHDRV-to-BOOTLO resistor			250	kΩ	
t <sub>r</sub> /t <sub>f</sub> Rise and fall time (see Notes 2 and 3)	C <sub>L</sub> = 3.3 nF, V(BOOTLO) = GND, T <sub>J</sub> = 125°C	V(BOOT) = 4 V		85	ns
		V(BOOT) = 8 V		70	
		V(BOOT) = 14 V		65	
	C <sub>L</sub> = 10 nF, V(BOOTLO) = GND, T <sub>J</sub> = 125°C	V(BOOT) = 4 V		170	
		V(BOOT) = 8 V		140	
		V(BOOT) = 14 V		100	
t <sub>PHL</sub> Propagation delay time, HIGHDR going low (excluding deadtime)	V(BOOTLO) = GND, T <sub>J</sub> = 125°C, See Notes 2 and 3	V(BOOT) = 4 V		120	ns
		V(BOOT) = 8 V		100	
		V(BOOT) = 14 V		80	

NOTES: 2: Ensured by design, not production tested.

3. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the r<sub>DS(on)</sub> of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

**electrical characteristics over recommended operating virtual junction temperature range,  
 $V_{CC} = 12\text{ V}$ ,  $\text{ENABLE} = \text{High}$ ,  $C_L = 3.3\text{ nF}$  (unless otherwise noted) (continued)**

**low-side driver**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output current	$V_{(\text{VDRV})} = 4\text{ V}$ , $T_J = 25^\circ\text{C}$ , See Note 2	$V_{(\text{LOWDR})} = 0.5\text{ V (src)}$	1	1.6		A
		$V_{(\text{LOWDR})} = 4\text{ V (sink)}$	2	2.4		
	$V_{(\text{VDRV})} = 8\text{ V}$ , $T_J = 25^\circ\text{C}$ , See Note 2	$V_{(\text{HIGHDR})} = 0.5\text{ V (src)}$	2	2.4		
		$V_{(\text{HIGHDR})} = 8\text{ V (sink)}$	2	3.3		
	$V_{(\text{VDRV})} = 14\text{ V (src)}$ , $T_J = 25^\circ\text{C}$ , See Note 2	$V_{(\text{HIGHDR})} = 0.5\text{ V (src)}$	2	3.9		
		$V_{(\text{HIGHDR})} = 14\text{ V (sink)}$	2	4.4		
$r_o$ Output resistance	$V_{(\text{VDRV})} = 4.5\text{ V}$ , $T_J = 25^\circ\text{C}$	$V_{(\text{LOWDR})} = 4\text{ V (src)}$			30	$\Omega$
		$V_{(\text{LOWDR})} = 0.5\text{ V (sink)}$			8	
	$V_{(\text{VDRV})} = 7.5\text{ V}$ , $T_J = 25^\circ\text{C}$	$V_{(\text{LOWDR})} = 7\text{ V (src)}$			25	
		$V_{(\text{LOWDR})} = 0.5\text{ V (sink)}$			7	
	$V_{(\text{VDRV})} = 11.5\text{ V}$ , $T_J = 25^\circ\text{C}$	$V_{(\text{LOWDR})} = 11\text{ V (src)}$			22	
		$V_{(\text{LOWDR})} = 0.5\text{ V (sink)}$			6	
LOWDR-to-PGND resistor				250		k $\Omega$
$t_r/t_f$ Rise and fall time	$C_L = 3.3\text{ nF}$ , $T_J = 125^\circ\text{C}$ , See Note 2	$V_{(\text{VDRV})} = 4\text{ V}$			60	ns
		$V_{(\text{VDRV})} = 8\text{ V}$			50	
		$V_{(\text{VDRV})} = 14\text{ V}$			40	
	$C_L = 10\text{ nF}$ , $T_J = 125^\circ\text{C}$ , See Note 2	$V_{(\text{VDRV})} = 4\text{ V}$			110	
		$V_{(\text{VDRV})} = 8\text{ V}$			100	
		$V_{(\text{VDRV})} = 14\text{ V}$			80	
$t_{\text{PLH}}$ Propagation delay time, LOWDR going high (excluding deadtime)	$T_J = 125^\circ\text{C}$ , See Notes 2 and 3	$V_{(\text{VDRV})} = 4\text{ V}$			110	ns
		$V_{(\text{VDRV})} = 8\text{ V}$			90	ns
		$V_{(\text{VDRV})} = 14\text{ V}$			80	ns

NOTES: 2: Ensured by design, not production tested.

3: The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the  $r_{\text{DS(on)}}$  of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

**$V_{CC}$  undervoltage lockout**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold voltage					10.3	V
Stop threshold voltage			7.5			V
$V_{\text{hys}}$	Hysteresis voltage		1	1.5		V
$t_{\text{pd}}$	Propagation delay time	50-mV overdrive, See Note 2		300	1000	ns
$t_d$	Falling-edge delay time	See Note 2	2		5	us

NOTE 2: Ensured by design, not production tested.

electrical characteristics over recommended operating virtual junction temperature range,  
 $V_{CC} = 12\text{ V}$ , ENABLE = High,  $C_L = 3.3\text{ nF}$  (unless otherwise noted) (continued)

**digital control (IN, ENABLE, SYNC)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH}$	High-level input voltage	IN	Over full $V_{CC}$ range			V
		ENABLE, SYNC	Over full $V_{CC}$ range			V
$V_{IL}$	Low-level input voltage	IN	Over full $V_{CC}$ range			V
		ENABLE, SYNC	Over full $V_{CC}$ range			V
ENABLE propagation delay time		See Note 2	2		7	$\mu\text{s}$

NOTE 2: Ensured by design, not production tested.

**thermal shutdown**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal shutdown		See Note 2	155	170	185	$^{\circ}\text{C}$
$t_d$	Falling edge delay time	See Note 2	10		20	$\mu\text{s}$

NOTE 2: Ensured by design, not production tested.

**drive regulator**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Recommended output voltage			4		14	V
$V_O$	Output voltage	$V_{CC} = 10\text{ V to }15\text{ V}$ , $I_O = 5\text{ mA to }150\text{ mA}$	-2		2	%nom
$V_{ref}$	Reference voltage	$V_{CC} = 10\text{ V to }15\text{ V}$		1.235		V
Dropout voltage		$V_{CC} = 10\text{ V}$ , See Note 2 $I_O = 150\text{ mA}$		1000	1100	mV
Line regulation		$V_{CC} = 10\text{ V to }15\text{ V}$ , $I_O = 5\text{ mA}$		0.2		%/V
Load regulation		$V_{CC} = 10\text{ V}$ , $I_O = 5\text{ mA to }150\text{ mA}$		2		%
Current limit		$V_{CC} = 8\text{ V}$		0.5	0.6	A
PWRRDY saturation voltage		$I_O = 5\text{ mA}$			0.8	V
$I_{lkg}$	Leakage current	$V_I(\text{PWRRDY}) = 4.5\text{ V}$			1	$\mu\text{A}$

**drive regulator undervoltage lockout**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold voltage		See Note 2			85	%Vref
Stop threshold voltage		See Note 2	80			%Vref
$V_{hys}$	Hysteresis voltage	See Note 2	2.5	5		%Vref
$t_{pd}$	Propagation delay time	50-mV overdrive, See Note 2		300	1000	ns
Falling-edge delay time		See Note 2	2		5	$\mu\text{s}$
Power on reset time		See Note 2		100	1000	$\mu\text{s}$

NOTE 2: Ensured by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

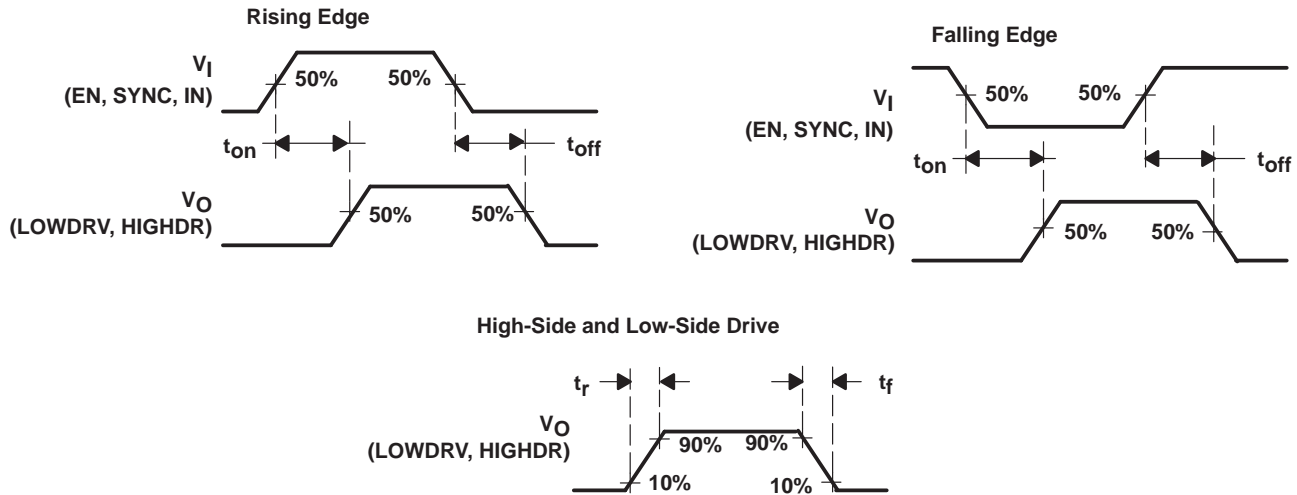


Figure 1. Voltage Waveforms

TYPICAL CHARACTERISTICS

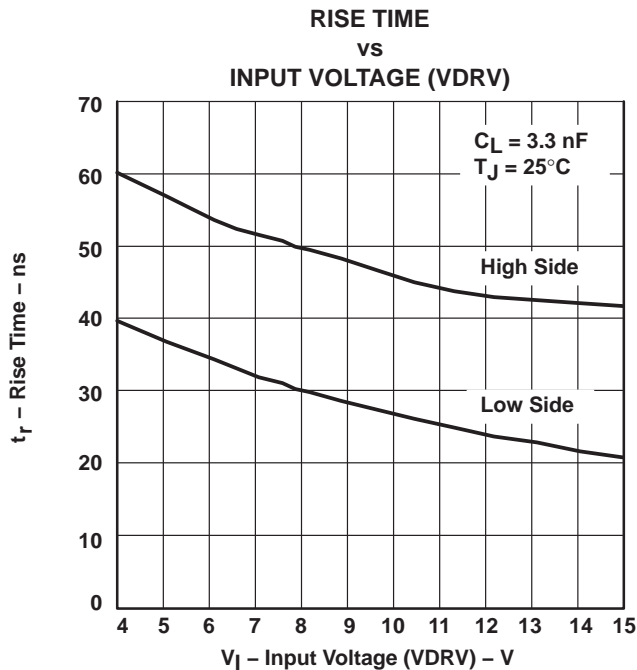


Figure 2

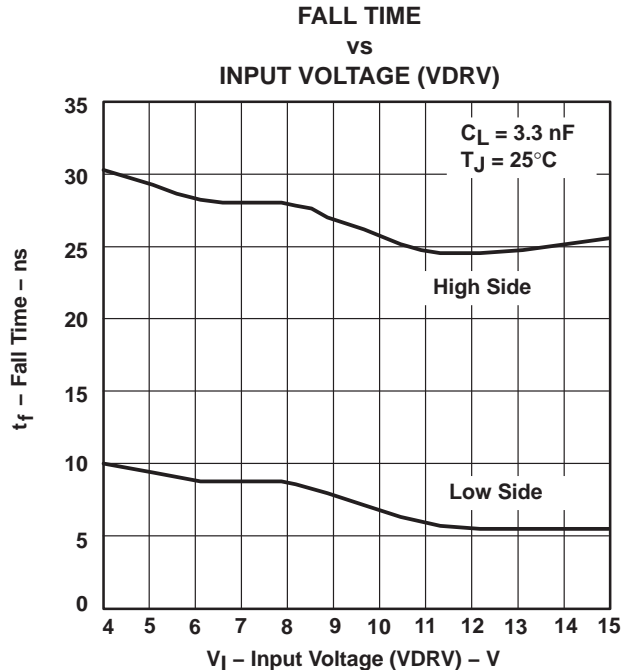
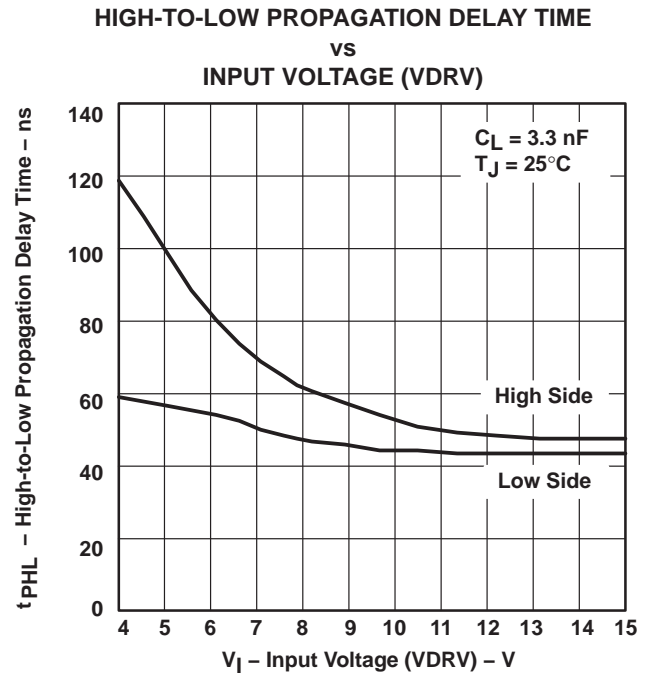
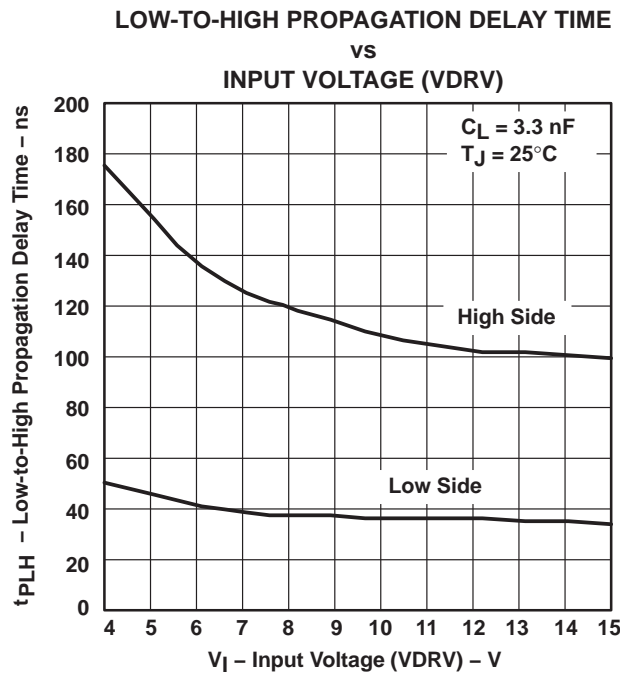
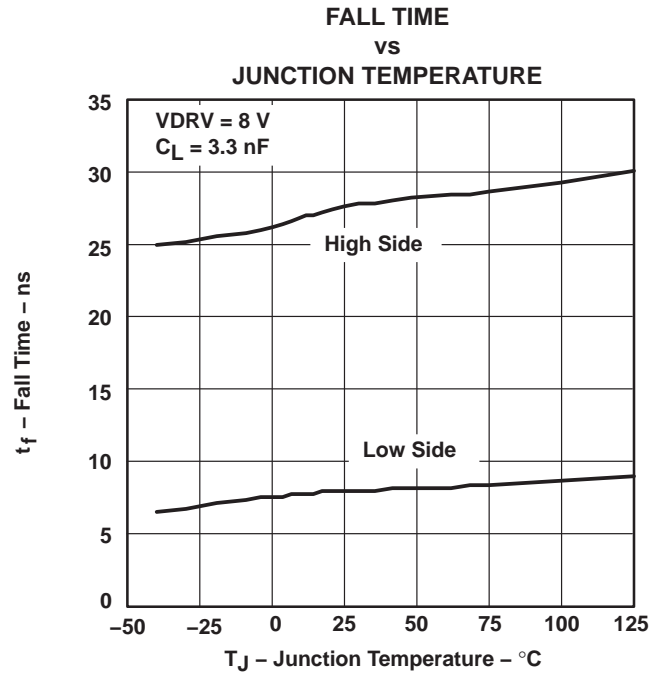
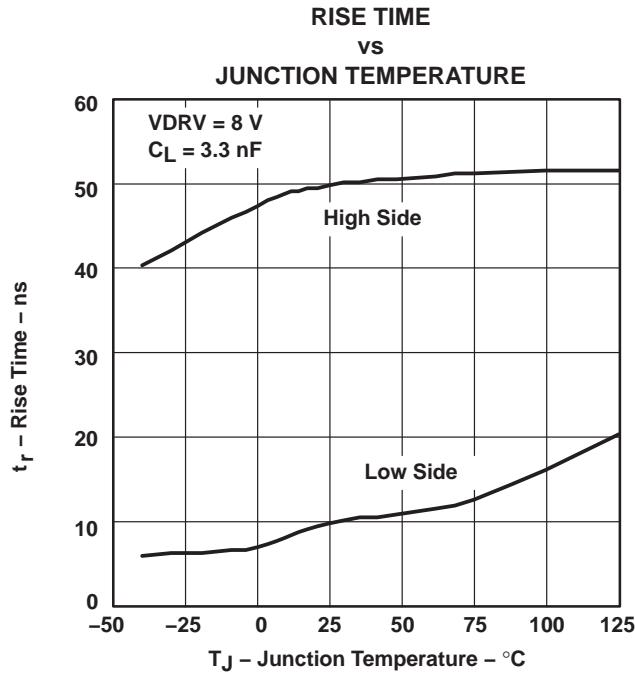


Figure 3

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY TIME  
vs  
JUNCTION TEMPERATURE

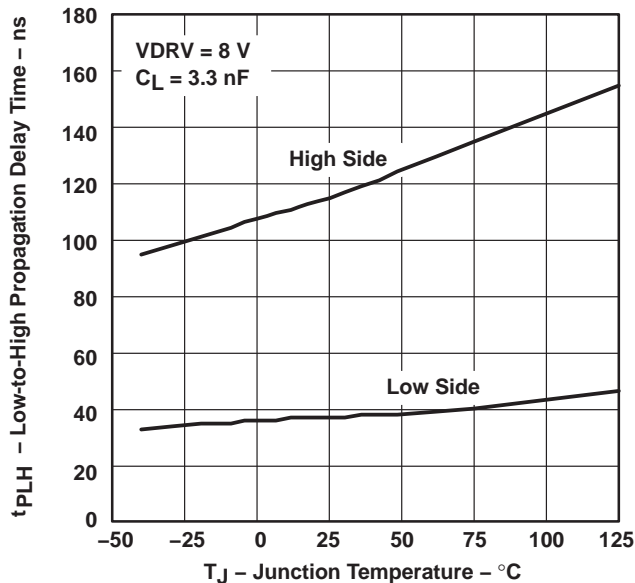


Figure 8

HIGH-TO-LOW PROPAGATION DELAY TIME  
vs  
JUNCTION TEMPERATURE

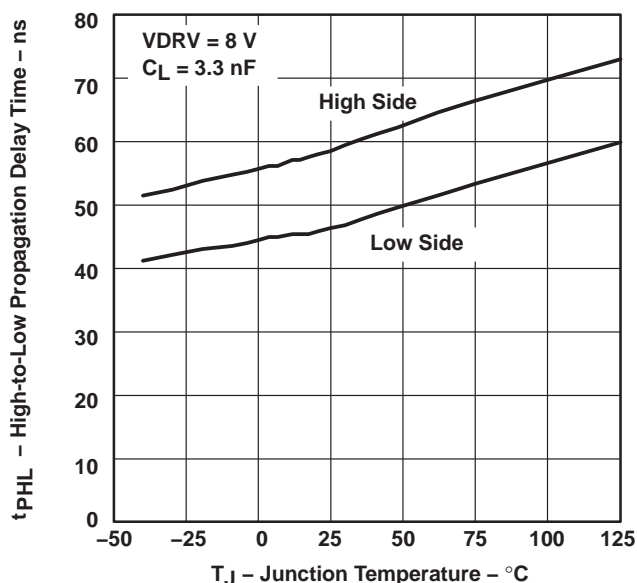


Figure 9

DRIVER-OUTPUT RISE TIME  
vs  
LOAD CAPACITANCE

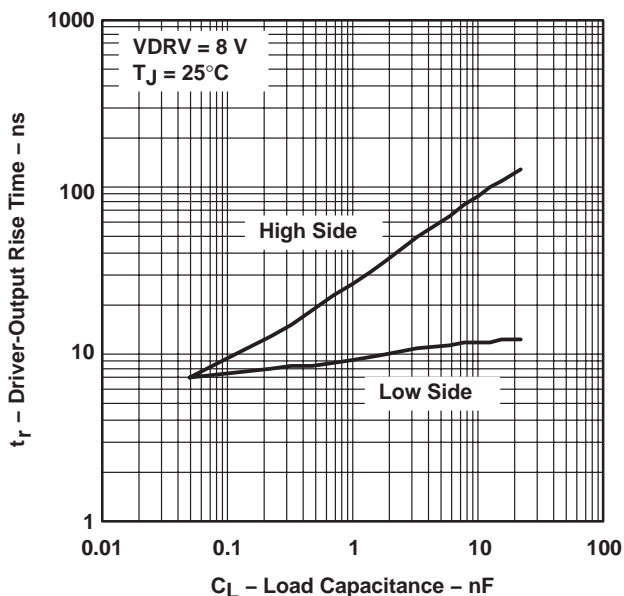


Figure 10

DRIVER-OUTPUT FALL TIME  
vs  
LOAD CAPACITANCE

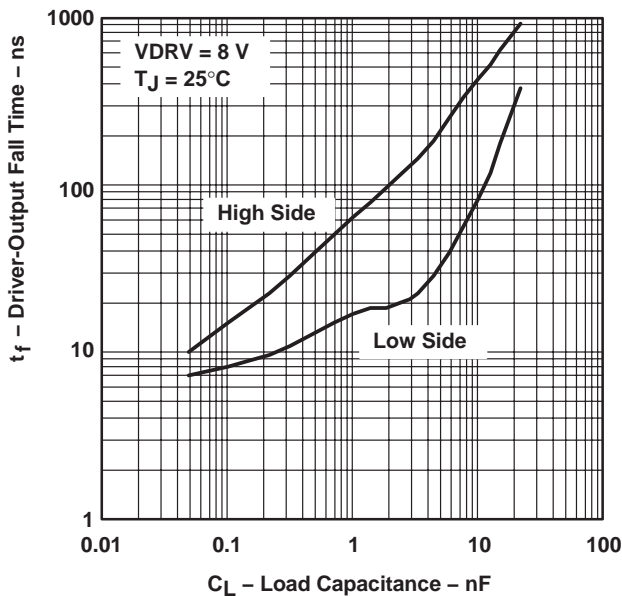


Figure 11

TYPICAL CHARACTERISTICS

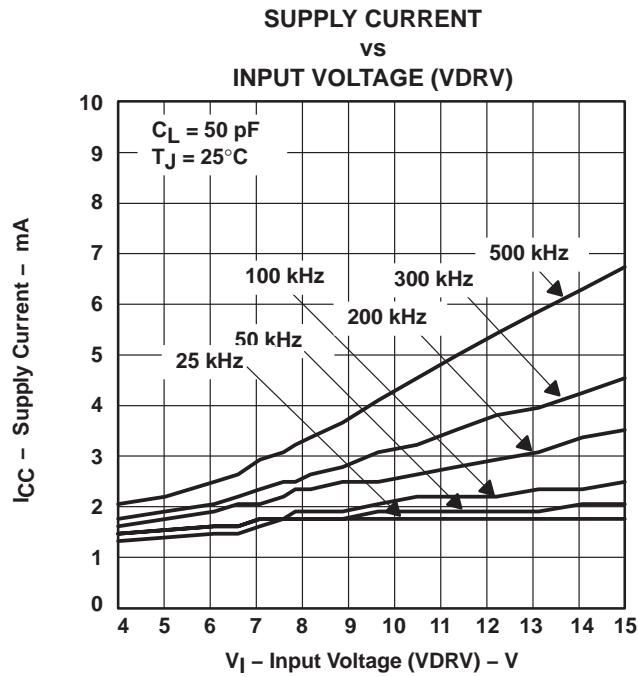


Figure 12

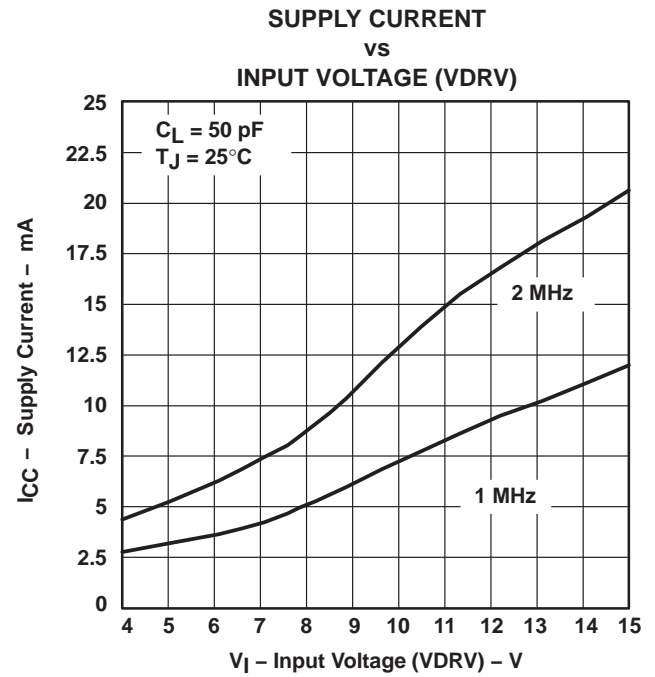


Figure 13

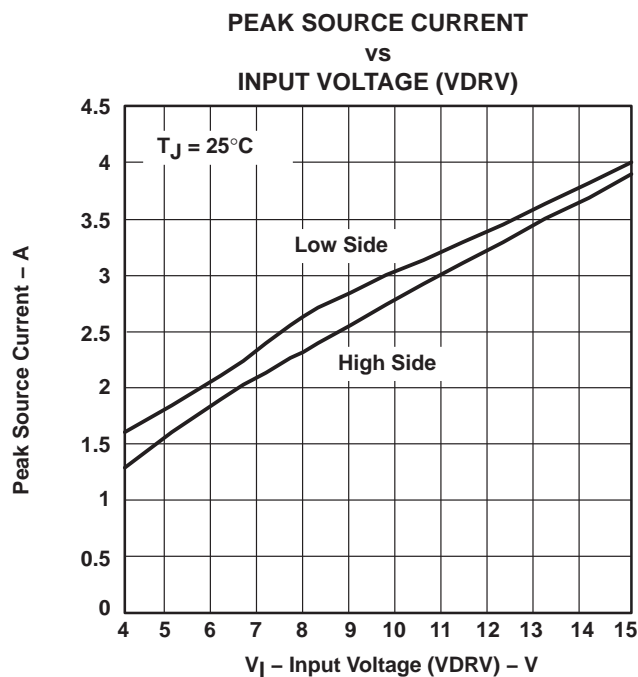


Figure 14

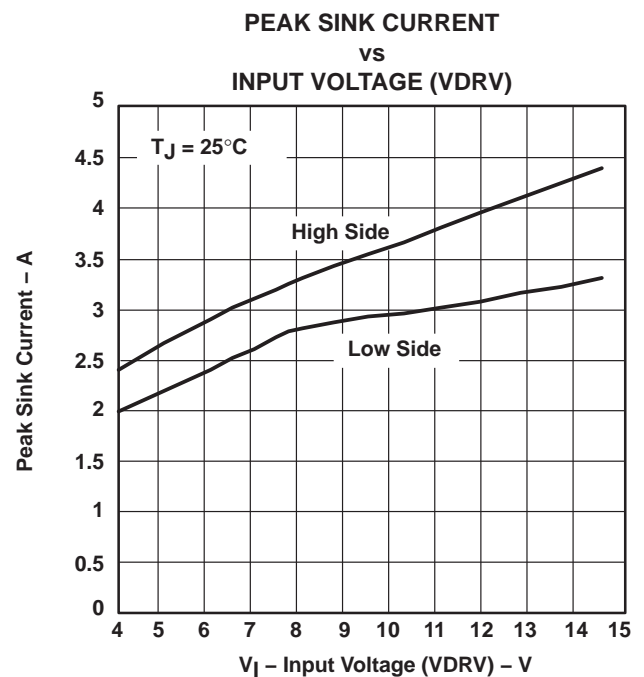


Figure 15

TYPICAL CHARACTERISTICS

START/STOP  $V_{CC}$  UNDERVOLTAGE LOCKOUT  
vs  
JUNCTION TEMPERATURE

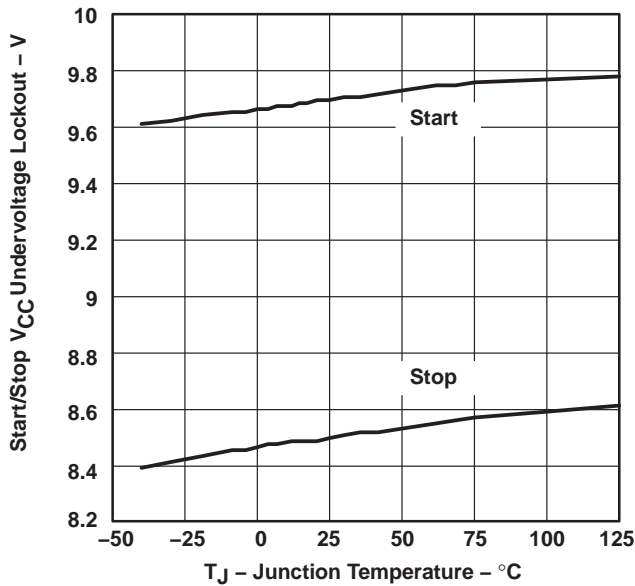


Figure 16

BOOTSTRAP SCHOTTKY DIODE  
INPUT CURRENT  
vs  
OUTPUT VOLTAGE

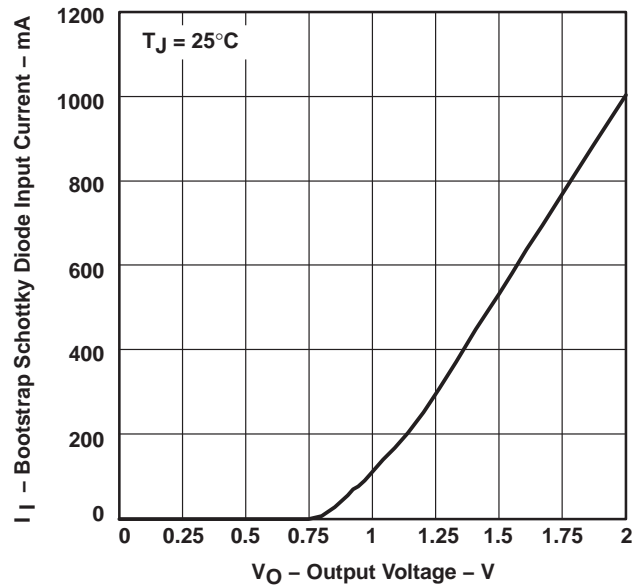


Figure 17

DELAY TIME (DEAD TIME)  
vs  
INPUT VOLTAGE (VDRV)

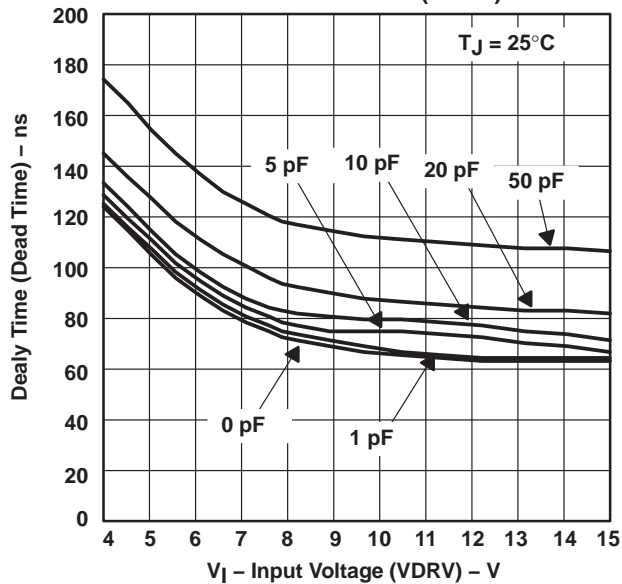


Figure 18

DELAY TIME  
vs  
JUNCTION TEMPERATURE

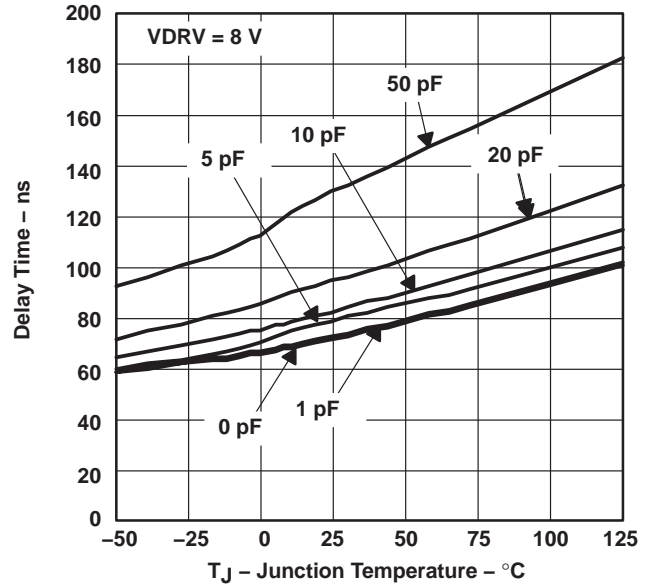


Figure 19

TYPICAL CHARACTERISTICS

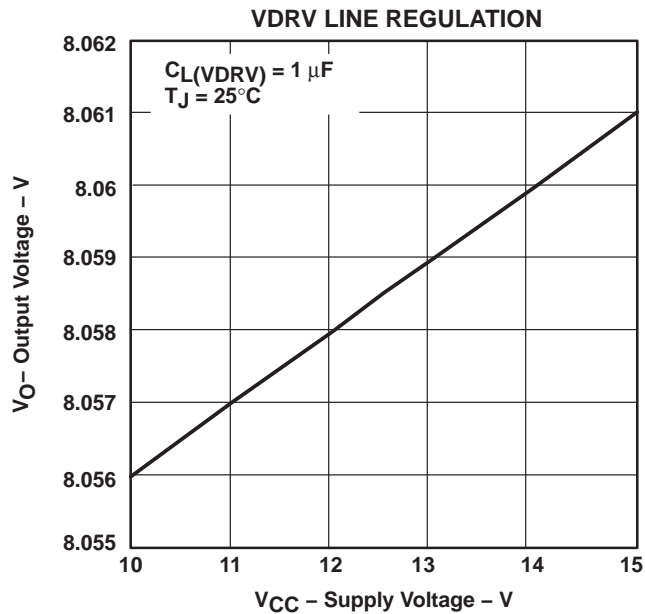


Figure 20

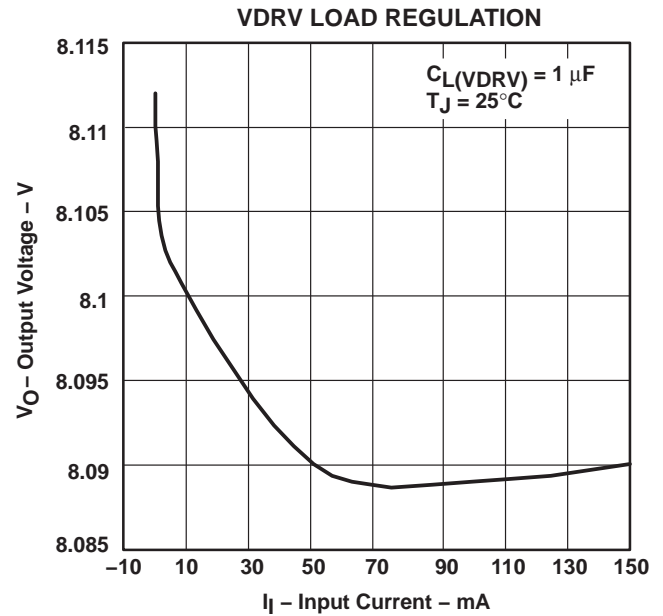
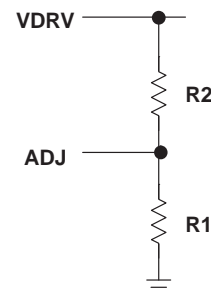


Figure 21

APPLICATION INFORMATION

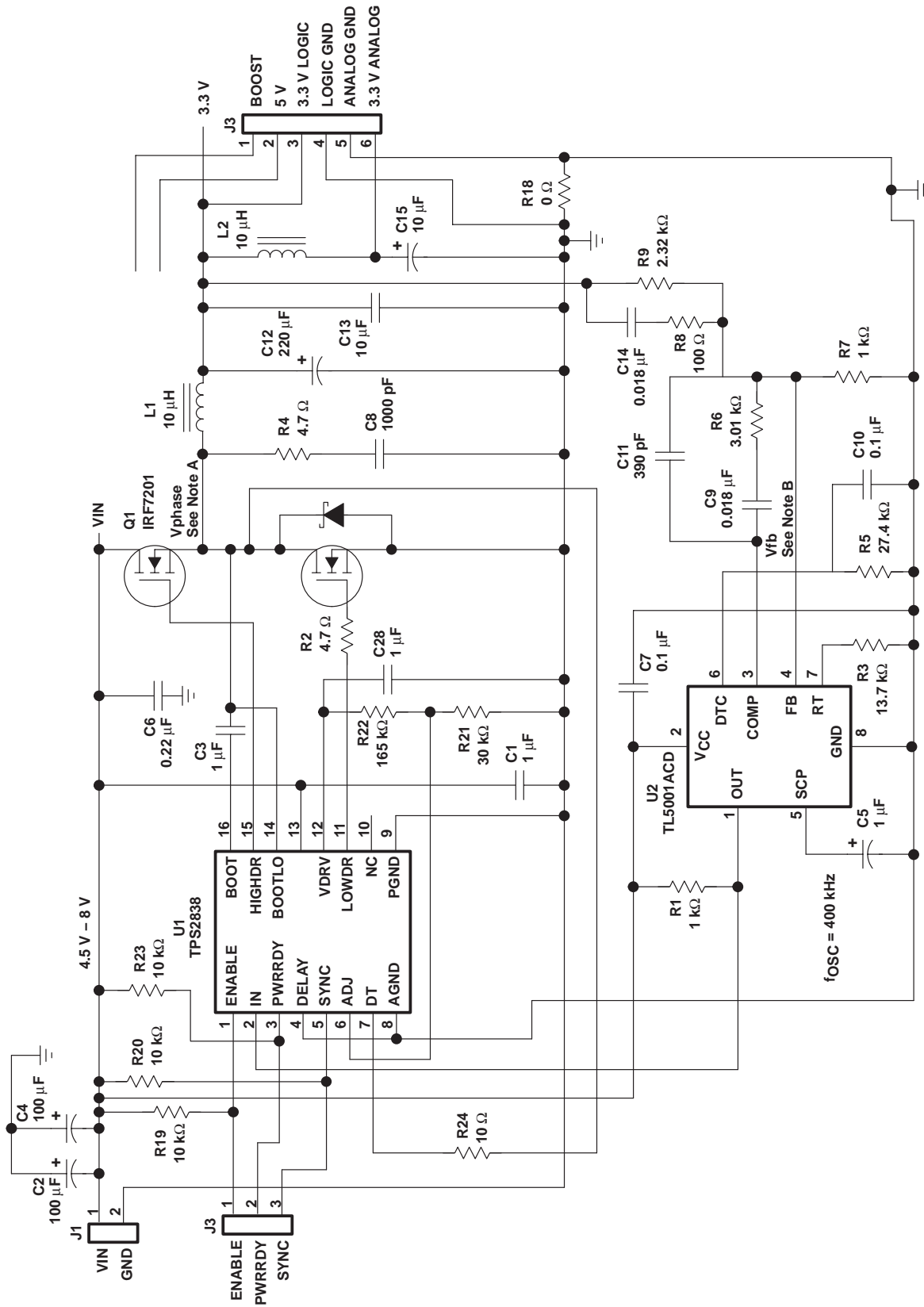
Figure 22 shows the circuit schematic of a 100-kHz synchronous-buck converter implemented with a TL5001ACD pulse-width-modulation (PWM) controller and a TPS2838 driver. The converter operates over an input range from 4.5 V to 12 V and has a 3.3-V output. The circuit can supply 3-A continuous load. The converter achieves an efficiency of 94% for V<sub>IN</sub> = 5 V, I<sub>L</sub> = 1 A, and 93% for V<sub>IN</sub> = 5 V, I<sub>L</sub> = 3 A.

R1 (kΩ)	R2 (kΩ)	VDRV Voltage (V)
30	67	4
30	91	5
30	165	8
30	261	12
30	322	14.5



To set the regulator voltage (TPS2838/39) use the following equation:

$$R2 = \left( \frac{R1}{1.235} \times VDRV \right) - R1$$



NOTES:  
A. Node Vphase generates RFI. Make this as contained as possible.  
B. Node Vphase is very sensitive. Make this as short as possible.

Figure 22. 3.3-V 3-A Synchronous-Buck Converter Circuit

## APPLICATION INFORMATION

Great care should be taken when laying out the PC board. The power-processing section is the most critical and will generate large amounts of EMI if not properly configured. The junction of Q1, Q2, and L1 should be very tight. The connection from Q1 drain to the positive sides of C5, C10, and C11 and the connection from Q2 source to the negative sides of C5, C10, and C11 should be as short as possible. The negative terminals of C7 and C12 should also be connected to Q2 source.

Next, the traces from the MOSFET driver to the power switches should be considered. The BOOTLO signal from the junction of Q1 and Q2 carries the large gate drive current pulses and should be as heavy as the gate drive traces. The bypass capacitor (C14) should be tied directly across  $V_{CC}$  and PGND.

The next most sensitive node is the FB node on the controller (terminal 4 on the TL5001A). This node is very sensitive to noise pickup and should be isolated from the high-current power stage and be as short as possible. The ground around the controller and low-level circuitry should be tied to the power ground as the output. If these three areas are properly laid out, the rest of the circuit should not have other EMI problems and the power supply will be relatively free of noise.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2838PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TPS2838	<a href="#">Samples</a>
TPS2848PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TPS2848	<a href="#">Samples</a>
TPS2849PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TPS2849	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

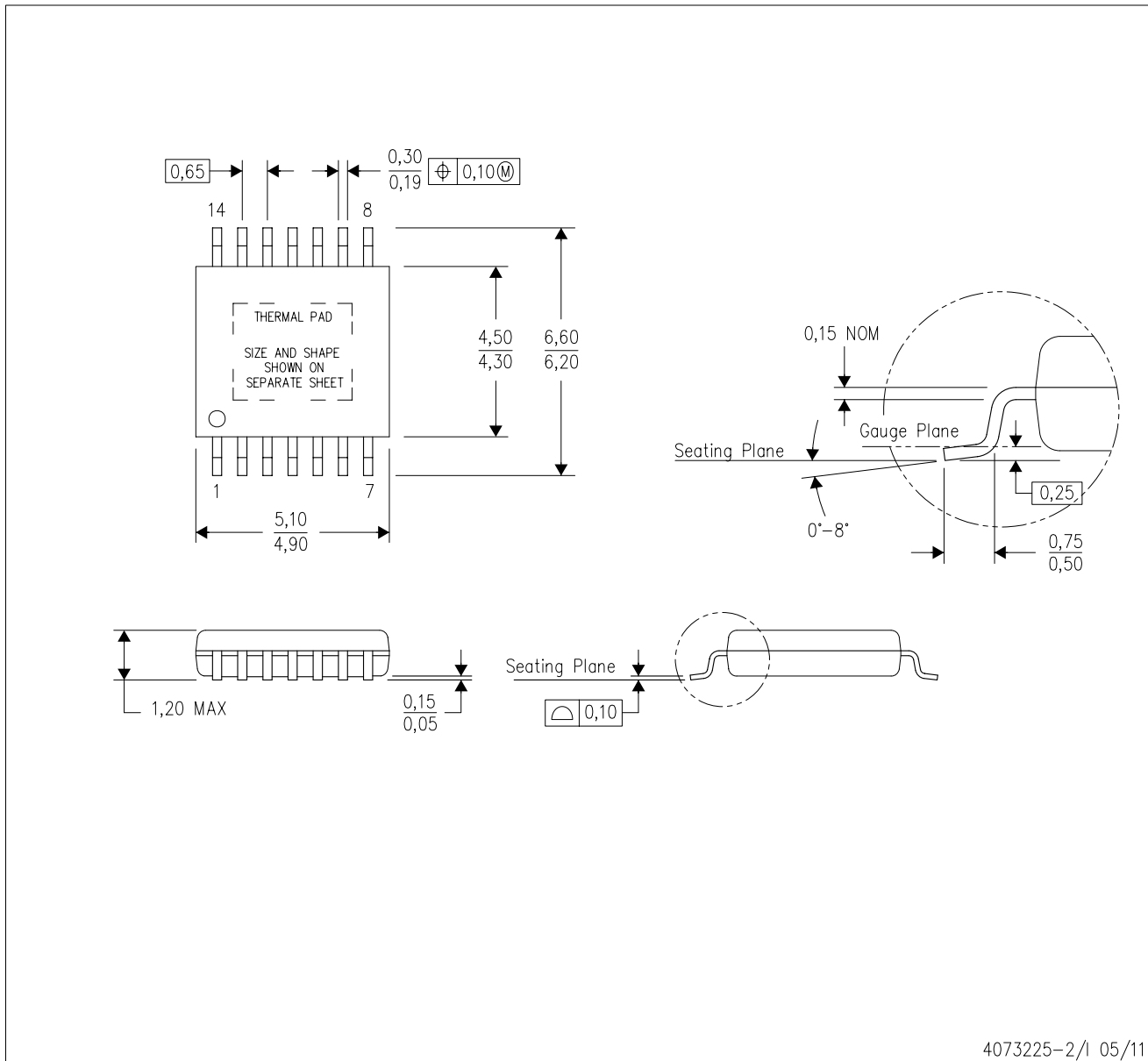
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PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-2/1 05/11

- NOTES:
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  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

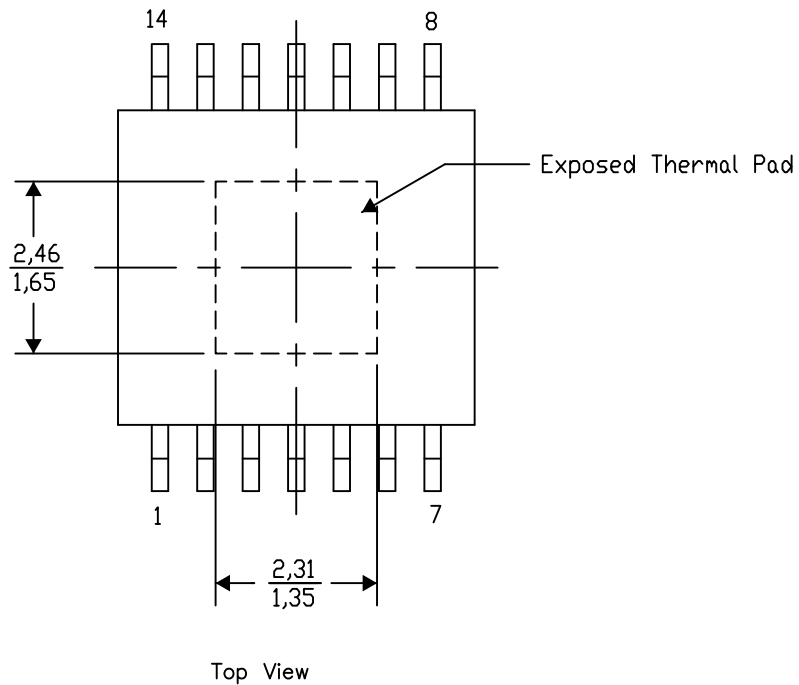
PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

**THERMAL INFORMATION**

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

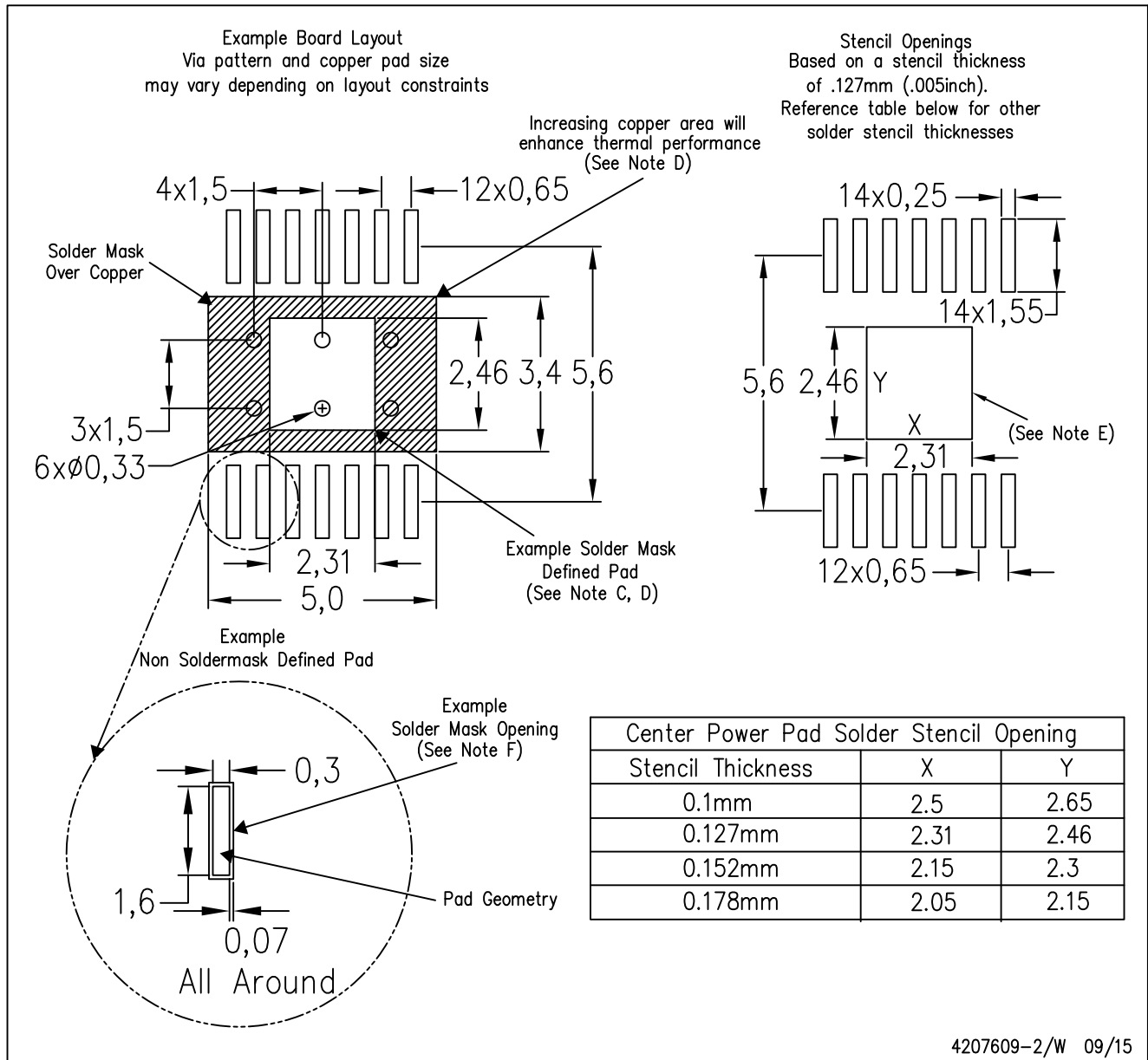
4206332-2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

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PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
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  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# THERMAL PAD MECHANICAL DATA

PWP (R-PDSO-G14)

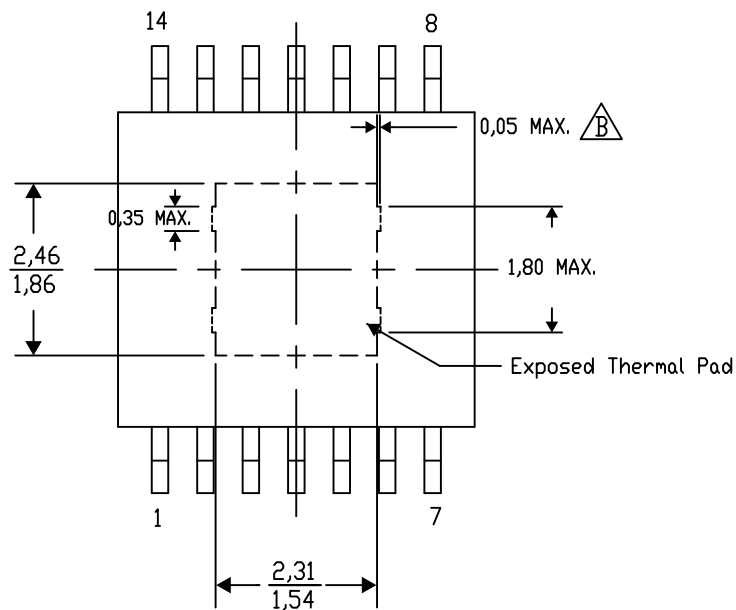
PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

4206332-44/AO 01/16

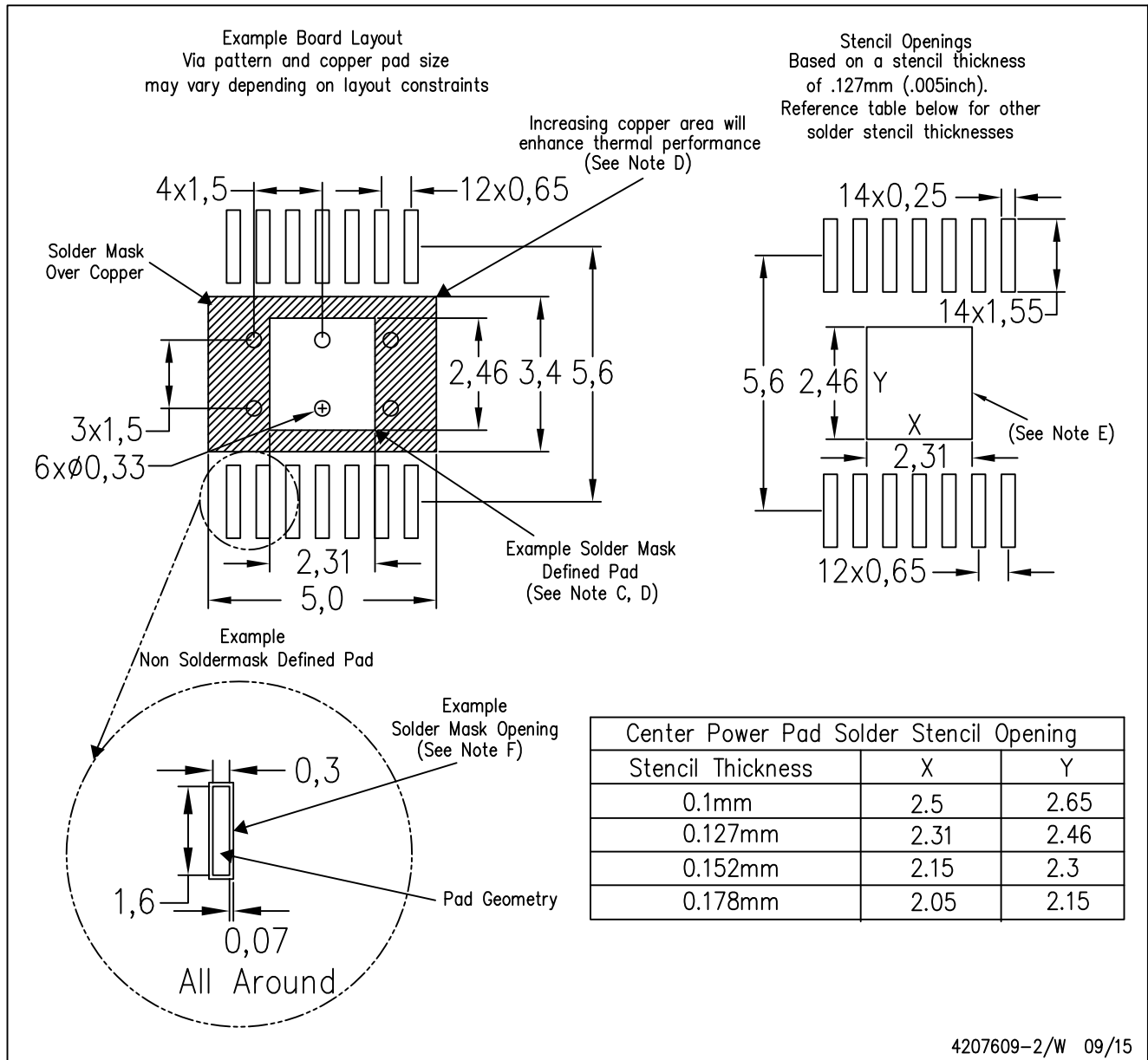
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

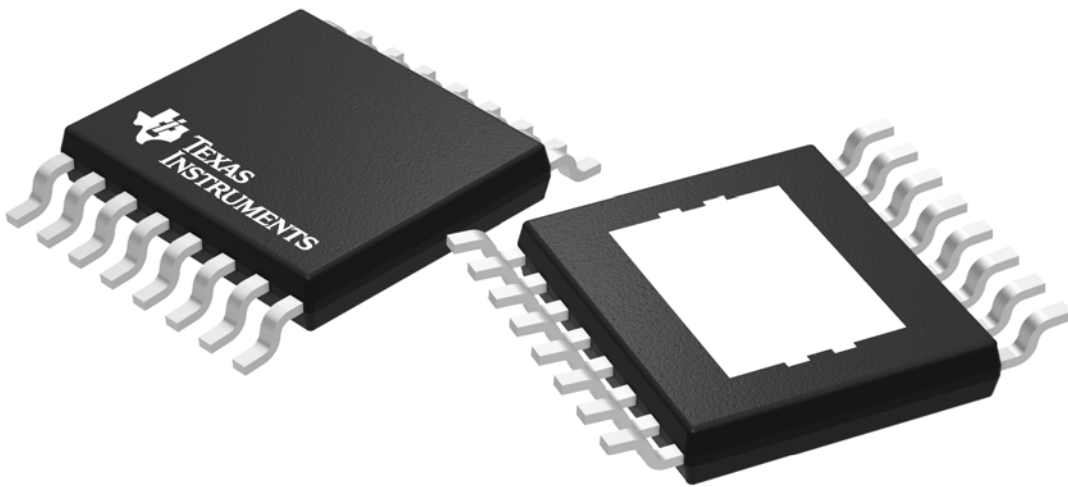
PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



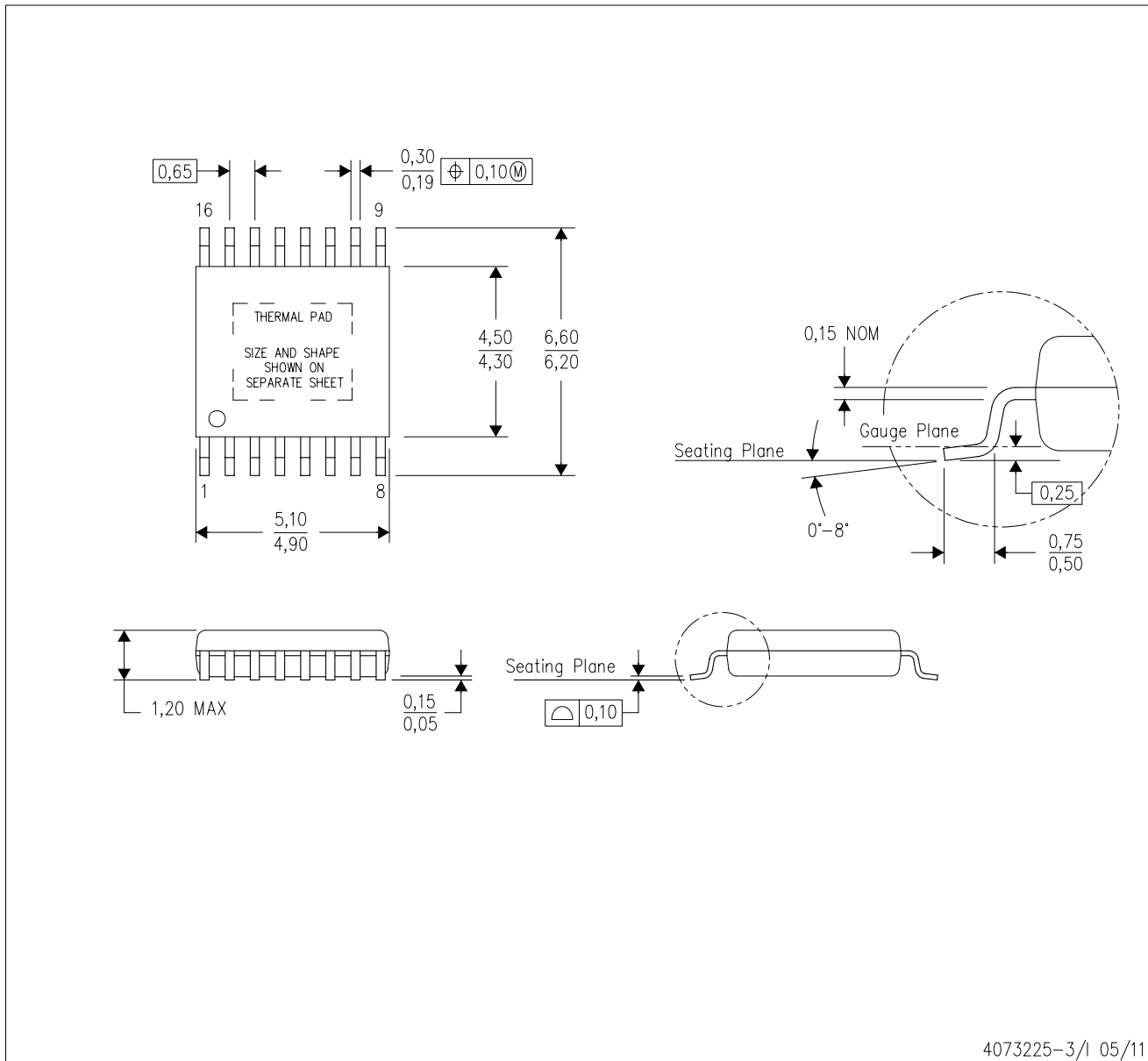
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
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  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

PWP (R-PDSO-G16)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-3/1 05/11

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  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

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# THERMAL PAD MECHANICAL DATA

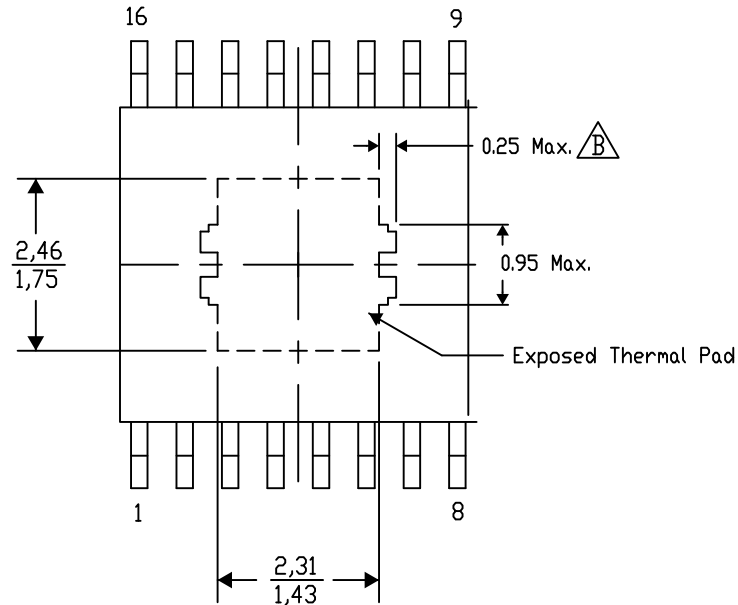
## PWP (R-PDSO-G16) PowerPAD™ SMALL PLASTIC OUTLINE

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

4206332-6/AO 01/16

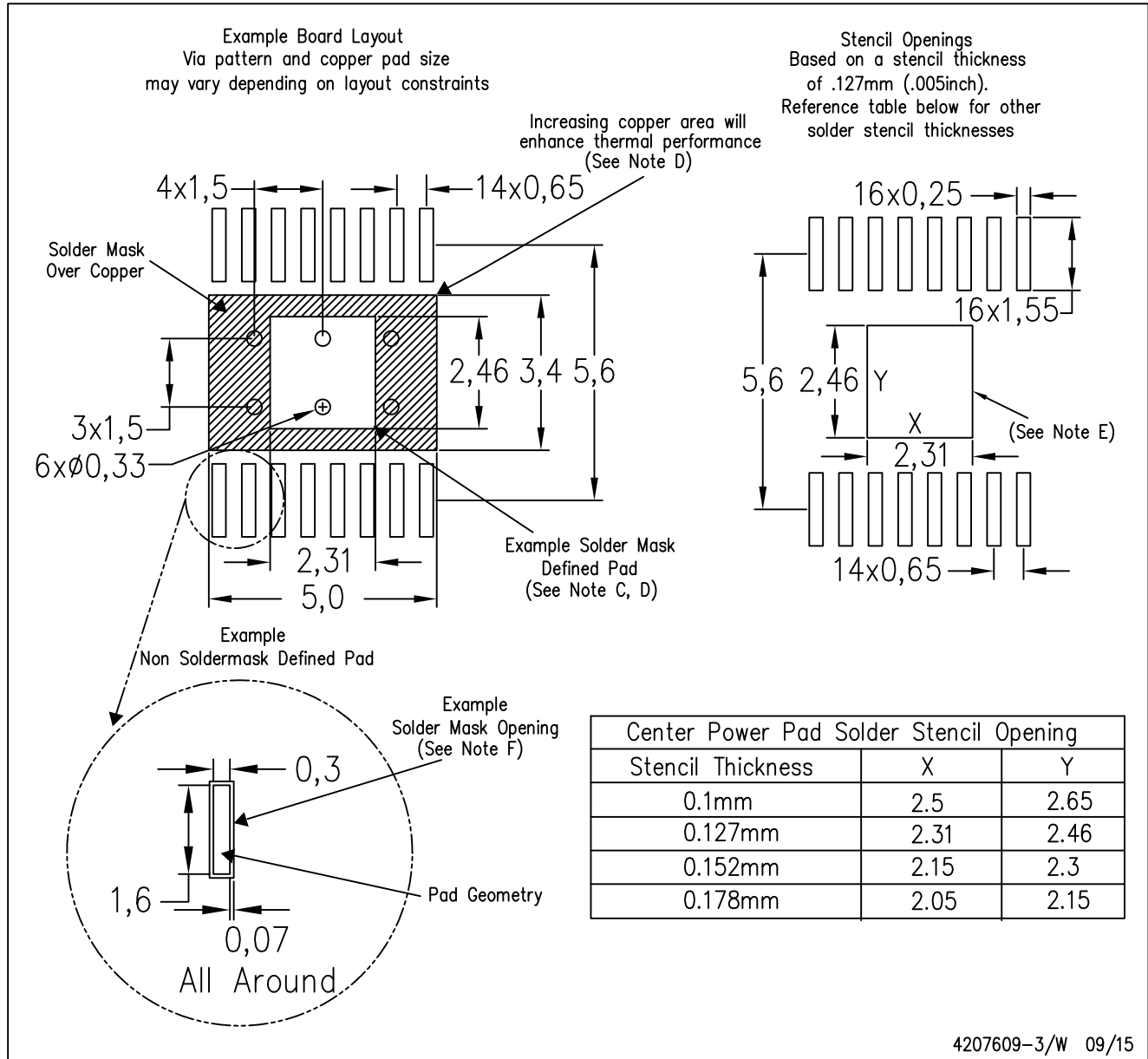
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

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PWP (R-PDSO-G16)

PowerPAD™ PLASTIC SMALL OUTLINE



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  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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